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【DOCKET】 Specification 1

【DOCKET】 Drawings 1

【DOCKET】 Abstract 1

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[Title of the Document] Claim

[Claim 1]

A semiconductor memory card comprising:

a host interface for sending and receiving control signals and data to and from an access device located outside of the semiconductor memory card;

a nonvolatile memory formed of a plurality of sectors, of which 2 to *i*-th power pieces of continuous sectors (*i* is a positive integer) are grouped into a block as a minimum unit for data erasing;

a memory controller for controlling erasing, writing, and reading of data for said nonvolatile memory; and

a first memory including a card information storage part which stores information on characteristics of the semiconductor memory card such as data access performance of said nonvolatile memory.

[Claim 2]

The semiconductor memory card according to claim 2, wherein said card information storage part stores at least one of information on internal physical characteristics of said semiconductor memory card, information on access conditions for access to said semiconductor memory card, information on access performance of said semiconductor memory card such as transfer rate, and information on

abnormal process of said semiconductor memory card such as incidence of error.

[Claim 3]

The semiconductor memory card according to claim 2, wherein, in response to a request of said access device, said semiconductor memory card transmits information on access conditions for fastest access to said semiconductor memory card and information on access performance associated with access to said semiconductor memory card under said access conditions to said access device.

[Claim 4]

The semiconductor memory card according to claim 2, wherein, in response to information on access conditions designated by said access device, said semiconductor memory card transmits information on access performance associated with access to said semiconductor memory card under said access conditions to said access device.

[Claim 5]

The semiconductor memory card according to claim 2, wherein, in response to information on access performance designated by said access device, said semiconductor memory card transmits information on semiconductor memory card

access conditions required to fulfill said access performance to said access device.

[Claim 6]

The semiconductor memory card according to claim 2, wherein, in response to information on access conditions designated by said access device and information on access performance, said semiconductor memory card determines whether or not said access performance is fulfilled when accessing to said semiconductor memory card under said access conditions and transmits a determination result to said access device.

[Claim 7]

The semiconductor memory card according to one of claims 2 to 6, wherein, instead of said access performance value or in addition to said access performance value, a flag representing rate performance of said semiconductor memory card is used.

[Claim 8]

The semiconductor memory card according to one of claims 2 to 6, wherein, instead of said access performance value or in addition to said access performance value, a flag representing power consumption in said semiconductor

memory card is used.

[Claim 9]

The semiconductor memory card according to claim 2, wherein a table bearing at least information on access performance of said semiconductor memory card is stored in said card information storage part and said table is transmitted to said access device thereby to allow calculation of access performance value on the basis of said table in said access device.

[Claim 10]

The semiconductor memory card according to claim 2, wherein a table bearing access performance value of said semiconductor memory card is stored in said card information storage part and said table is transmitted to said access device thereby to allow recognition of access performance of said semiconductor memory card in said access device.

[Claim 11]

An access device for accessing a semiconductor memory card provided with a plurality of sectors, of which 2 to i-th power pieces of continuous sectors (i is a positive integer) are grouped into a block as a minimum unit for

data erasing and in which stored data is managed according to a file system, comprising:

a slot for attachment of said semiconductor memory card;

a card information acquisition part for acquiring information on characteristics of said semiconductor memory card attached to said slot from said semiconductor memory card;

a card use condition storage part for storing information on access conditions which can be used when said access device accesses said semiconductor memory card and information on access performance required of said semiconductor memory card;

an access condition determination part for determining access conditions on the basis of information on the characteristics of said semiconductor memory card acquired by said card information acquisition part and information stored in said card use condition storage part;

a file system control part for acquiring access conditions determined by said access condition determination part and performing file access suitable for said access conditions; and

an access control part for accessing said semiconductor memory card in response to an access request from said file system control part.

[Claim 12]

The access device according to claim 11, wherein said access condition determination part determines, as said access condition, access unit size best suited to accessing said semiconductor memory card.

[Claim 13]

The access device according to claim 12, wherein said file system control part, when recording file data on said semiconductor memory card, determines continuous free areas of a length of multiples of said access unit size starting from an address of a length of multiples of said access unit size on the basis of management information of a file system constructed on said semiconductor memory card, and records the file data in said determined area on said semiconductor memory card.

[Claim 14]

The access device according to claim 12, wherein, when recording new file management information on said semiconductor memory card, said file system control part, after confirming that another file management information is recorded in the area of a length of multiples of said access unit size starting from an address of a length of

multiples of said access unit size and that a free area for writing new file management information exists on the basis of management information of a file system constructed on said semiconductor memory card, determines said free area as a position for writing of file management information, and records the file management information in said determined free area on said semiconductor memory card.

[Claim 15]

The access device according to claim 12, wherein, on the basis of management information of a file system constructed on said semiconductor memory card, said file system control part, when areas of said access unit size starting from an address of a length of multiples of said access unit size are partially used, effects merging with another area partially used to increase the number of areas in which the whole of the areas of said access unit size starting from an address of a length of multiples of said access unit size is the free area.

[Claim 16]

The access device according to claim 12, wherein said file system control part calculates a size of said area in which the whole of the areas of said access unit size starting from an address of a length of multiples of said

access unit size is the free area, and informs an application program of a value of the size as a free area length of said semiconductor memory card.

[Claim 17]

A semiconductor memory card comprising:

a nonvolatile memory; and

a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device,

wherein determination as to whether an invalid block of said nonvolatile memory is erased or not is made in accordance with a data writing start address and data size from said access device.

[Claim 18]

A semiconductor memory card comprising:

a nonvolatile memory;

a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device; and

a host information storage part,

wherein said host information storage part temporarily stores therein a data writing start address and data size transferred from an access device, and said

memory controller has a free block generating section for determining whether or not an invalid block of said nonvolatile memory is erased in accordance with the data writing start address and data size temporarily stored in said host information storage part.

[Claim 19]

The semiconductor memory card according to claim 18, wherein said free block generating section determines the number of erase blocks in accordance with the level of said data size.

[Claim 20]

The semiconductor memory card according to claim 19, wherein said nonvolatile memory is formed of at least two nonvolatile memory chips, and, during the time one of the nonvolatile memory chips is subjected to writing, an invalid block within the other nonvolatile memory chip is erased.

[Claim 21]

An access device connected to the semiconductor memory card set forth in claim 18 that transfers, in addition to a data writing command, a data writing start address and data size to said semiconductor memory card.

[Claim 22]

A semiconductor memory card comprising:

a plurality of nonvolatile memories; and

a memory controller for exercising reading-writing control over said nonvolatile memories in response to reading-writing instructions from an access device,

wherein, in response a speed mode (high-speed mode/low-speed mode) for writing to said nonvolatile memories specified by said access device, said memory controller controls timing at which time periods for writings to said nonvolatile memories overlap each other.

[Claim 23]

A semiconductor memory card comprising:

a plurality of nonvolatile memories;

a memory controller for exercising reading-writing control over said nonvolatile memories in response to reading-writing instructions from an access device; and

a host information storage part,

wherein said host information storage part stores therein a speed mode (high-speed mode/low-speed mode) for writing to said nonvolatile memories transferred from said access device, and said memory controller has a nonvolatile memory access section for performing parallel writing to

said nonvolatile memories,

and wherein said nonvolatile memory access section controls timing at which time periods for writings to said nonvolatile memories overlap each other in response the speed mode stored in said host information storage part.

[Claim 24]

An access device connected to the semiconductor memory card set forth in claim 22 that transfers, in addition to a data writing command, a speed mode (high-speed mode/low-speed mode) for writing to said nonvolatile memories to said semiconductor memory card.

[Claim 25]

A semiconductor memory card comprising:

a nonvolatile memory; and

a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device,

wherein said memory controller determines whether or not a logical address transferred by said access device is converted into a physical address of said nonvolatile memory in response to an instruction from said access device.

[Claim 26]

A semiconductor memory card comprising:

a nonvolatile memory;

a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device; and

a host information storage part,

wherein said host information storage part temporarily stores therein a logical-to-physical conversion through flag transferred from said access device, and said memory controller has a nonvolatile memory access section for converting a logical address transferred from said access device into a physical address when the logical-to-physical conversion through flag temporarily stored in said host information storage part is in an inactive state on one hand, and defining a logical address transferred from said access device as a physical address without performing logical-to-physical conversion when the logical-to-physical conversion through flag is in an active state on the other hand.

[Claim 27]

An access device connected to the semiconductor memory card set forth in claim 25 that transfers, in addition to a data writing command, a logical-to-physical

conversion through flag to said semiconductor memory card.

[Claim 28]

A semiconductor memory card comprising:

a nonvolatile memory; and

a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device,

wherein said memory controller generates a free block (erased block) in response to an instruction from the access device.

[Claim 29]

A semiconductor memory card comprising:

a nonvolatile memory;

a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device; and

a host information storage part,

wherein said memory controller has a free physical area generating section for detecting the remaining amount of free blocks (erased blocks) of said nonvolatile memory and the number of writing sectors of each physical block and, in response to the result of detection, issuing a defragmentation request signal to said access device.

[Claim 30]

The semiconductor memory card according to claim 29, wherein said host information storage part temporarily stores therein a defragmentation instruction flag transferred from said access device, and said free physical area generating section generates a free block (erased block) in said nonvolatile memory on the basis of said defragmentation instruction flag.

[Claim 31]

An access device connected to the semiconductor memory card set forth in claim 30 that transfers a defragmentation instruction flag to said semiconductor memory card to generate a free block (erased block) in said nonvolatile memory.

[Claim 32]

A semiconductor memory card comprising:

a nonvolatile memory; and

a memory controller which exercises reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device and has a volatile memory for storing therein address management information of said nonvolatile memory,

wherein said memory controller writes said address management information into said nonvolatile memory in response to an instruction from said access device.

[Claim 33]

A semiconductor memory card comprising:

a nonvolatile memory;

a memory controller which exercises reading-writing control over said nonvolatile memory in response to a reading-writing instruction from an access device and has a volatile memory for storing therein address management information of said nonvolatile memory; and

a host information storage part,

wherein said host information storage part temporarily stores therein an address management information update flag transferred from said access device, and said memory controller has a nonvolatile memory access section for controlling writing of user data transferred by said access device to said nonvolatile memory and writing said address management information to said nonvolatile memory when said address management information update flag is in an active state.

[Claim 34]

An access device connected to the semiconductor

memory card set forth in claim 33 that transfers an address management information update flag to said semiconductor memory card.

[Claim 35]

An access method for accessing a semiconductor memory card provided with a plurality of sectors, of which 2 to *i*-th power pieces of continuous sectors (*i* is a positive integer) are grouped into a block as a minimum unit for data erasing and in which stored data is managed according to a file system, comprising:

a card information acquisition step for acquiring information on characteristics of said loaded semiconductor memory card attached to a slot from said semiconductor memory card;

a card use condition storage step for storing information on access conditions which can be used when accessing said semiconductor memory card and information on access performance required of said semiconductor memory card;

an access condition determination step for determining access conditions on the basis of information on the characteristics of said semiconductor memory card acquired in said card information acquisition step and information stored in said card use condition storage step;

a file system control step for acquiring access conditions determined in said access condition determination step and performing file access suitable for said access conditions; and

an access control step for accessing said semiconductor memory card in response to an access request made in said file system control step.

[Claim 36]

The access method according to claim 35, wherein said access condition determination step is to determine, as said access condition, access unit size best suited to accessing said semiconductor memory card.

[Claim 37]

The access method according to claim 36, wherein said file system control step, when recording file data on said semiconductor memory card, determines continuous free areas of a length of multiples of said access unit size starting from an address of a length of multiples of said access unit size on the basis of management information of a file system constructed on said semiconductor memory card, and records the file data in said determined area on said semiconductor memory card.

[Claim 38]

The access method according to claim 36, wherein, when recording new file management information on said semiconductor memory card, said file system control step, after confirming that another file management information is recorded in the area of a length of multiples of said access unit size starting from an address of a length of multiples of said access unit size and that a free area for writing new file management information exists on the basis of management information of a file system constructed on said semiconductor memory card, determines said free area as a position for writing of file management information, and records the file management information in said determined free area on said semiconductor memory card.

[Claim 39]

The access method according to claim 36, wherein, on the basis of management information of a file system constructed on said semiconductor memory card, said file system control step, when the areas of said access unit size starting from an address of a length of multiples of said access unit size are partially used, effects merging with another area partially used to increase the number of areas in which the whole of the areas of said access unit size starting from an address of a length of multiples of

said access unit size is the free area.

[Claim 40]

The access method according to claim 36, wherein said file system control step is to calculate a size of said area in which the whole of the areas of said access unit size starting from an address of a length of multiples of said access unit size is the free area, and informs an application program of a value of the size as a free area length of said semiconductor memory card.

[Claim 41]

An access method whereby, with connection to the semiconductor memory card set forth in claim 18, in addition to a data writing command, a data writing start address and data size are transferred to said semiconductor memory card.

[Claim 42]

An access method whereby, with connection to the semiconductor memory card set forth in claim 22, in addition to a data writing command, a speed mode (high-speed mode/low-speed mode) for writing to a plurality of said nonvolatile memories is transferred to said semiconductor memory card.

[Claim 43]

An access method whereby, with connection to the semiconductor memory card set forth in claim 25, in addition to a data writing command, a logical-to-physical conversion through flag is transferred to said semiconductor memory card.

[Claim 44]

An access method whereby, with connection to the semiconductor memory card set forth in claim 30, a defragmentation instruction flag for generating a free block (erased block) in said nonvolatile memory is transferred to said semiconductor memory card.

[Claim 45]

An access method whereby, with connection to the semiconductor memory card set forth in claim 33, an address management information update flag is transferred to said semiconductor memory card.

[Title of the Document] DESCRIPTION

[Title of the Invention] SEMICONDUCTOR MEMORY CARD, ACCESS DEVICE, AND ACCESS METHOD

[Technical Field]

[0001]

The present invention relates to a semiconductor memory card, and an access device and an access method for accessing the semiconductor memory card.

[Background Art]

[0002]

There are various types of recording media, for example, magnetic disks, optical disks, and magneto-optical disks, that record digital data such as music contents and video data therein. Since a semiconductor memory card as a sort of the recording media uses a semiconductor memory such as a flash ROM as a recording device to miniaturize the recording media, the semiconductor memory card has been rapidly spreading especially in compact portable equipment such as a digital still camera and cellular phone terminal.

[0003]

Data stored in the semiconductor memory card is managed according to a file system and the user can easily handle the stored data as a file. Conventionally used file systems include a FAT file system (refer to Non-patent document 1 for details), UDF (Universal Disk Format) (refer

to Non-patent document 2 for details), and NTFS (New Technology File System). Since the semiconductor memory card in which the data is managed according to the file systems can share the file between equipments interpreting the same file system, data can be exchanged between the equipments.

[0004]

The file system manages an information recording area for recording data by dividing the recording area into sectors as minimum access units and clusters as sets of sectors, and manages one or more clusters as a file. A free area is allocated in units of clusters as the area in which the data contained in the file is stored and the data contained in the file is not necessarily stored in a consecutive area. When a file which is not stored in the consecutive area is read or written, there has been a problem that the reading-writing rate becomes lower as compared with the case where a file stored in a consecutive area is read or written since a seek operation occurs during the reading or writing.

[0005]

There has hitherto been proposed a method for controlling data writing so as to store data corresponding to 1 page of a manuscript in the consecutive area in an image processing device (refer to Patent document 1, for

example) as a method for solving the above-mentioned problems. In this conventional method, by necessarily writing data in a consecutive area having a fixed length in data writing, it can be secured that process can be certainly finished within a certain process time in data reading.

(Patent document 1) Japanese Unexamined Patent Publication JP-A 2002-29101

(Non-patent document 1) ISO/IEC 9293, "Information Technology-Volume and file structure of disk cartridges for information" (1994)

(Non-patent document 2) OSTA Universal Disk Format Specification Revision 1.50 (1997)

[Disclosure of the Invention]

[Problems to be solved by the Invention]

[0006]

The above mentioned conventional arts, however, have the following problem. In the conventional control method, data size for 1 page of the draft as process unit of the image processing device is used as a unit of consecutive area. That is, the unit of consecutive area is determined based on the size suitable for data to be handled by an application. This method is effective for the recording medium which causes no difference in writing rate due to distinction of writing unit to the recording medium.

However, in the semiconductor memory card, since the writing unit has a great influence on the writing rate and the relationship between the writing unit and writing rate varies depending on characteristics and management method of the semiconductor memory for use, an optimum access method for all semiconductor memory cards are not uniquely determined, and even when the data size is fixed as in the conventional example, it is impossible for all of the semiconductor memory cards to be accessed at high-rate.

[0007]

In consideration of said problem, the present invention is characterized by achieving high-rate access to the semiconductor memory card by holding information on access performance of the semiconductor memory card in the semiconductor memory card and by bringing efficiency to processes in either side of the access device or semiconductor memory card, or both of them, on the basis of the information.

[0008]

According to the first invention devised to solve the problem, there is provided a semiconductor memory card characterized in that a card information storage part for storing therein information on access performance of the semiconductor memory card is disposed to allow acquisition of a part or all of the information from an access device.

[0009]

According to the second invention devised to solve the problem, there is provided an access device characterized by acquiring information on semiconductor memory card's access performance from the semiconductor memory card and changing process contents of a file system on the basis of the acquired information in a file system control part incorporated therein.

[0010]

According to the third invention devised to solve the problem, there is provided a semiconductor memory card composed of a nonvolatile memory and a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from the access device. In the semiconductor memory card, determination as to whether an invalid block of the nonvolatile memory is erased or not is made in accordance with a data writing start address and data size from the access device.

[0011]

According to the fourth invention devised to solve the problem, there is provided a semiconductor memory card composed of a plurality of nonvolatile memories and a memory controller for exercising reading-writing control over said nonvolatile memories in response to reading-

writing instructions from the access device. In the semiconductor memory card, in response a speed mode (high-speed mode/low-speed mode) for writing to said nonvolatile memories specified by the access device, the memory controller controls timing at which time periods for writings to said nonvolatile memories overlap each other.

[0012]

According to the fifth invention devised to solve the problem, there is provided a semiconductor memory card composed of a nonvolatile memory and a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from the access device. In the semiconductor memory card, the memory controller determines whether or not a logical address transferred by the access device is converted into a physical address of the nonvolatile memory in response to a instruction from the access device.

[0013]

According to the sixth invention devised to solve the problem, there is provided a semiconductor memory card composed of a nonvolatile memory and a memory controller for exercising reading-writing control over said nonvolatile memory in response to a reading-writing instruction from the access device. In the semiconductor memory card, the memory controller generates a free block

(erased block) in response to an instruction from the access device.

[0014]

According to the seventh invention devised to solve the problem, there is provided a semiconductor memory card composed of a nonvolatile memory and a memory controller which exercises reading-writing control over said nonvolatile memory in response to a reading-writing instruction from the access device and has a nonvolatile memory for storing therein address management information of said nonvolatile memory. In the semiconductor memory card, the memory controller effects writing of said address management information into said nonvolatile memory in response to an instruction from the access device.

[Advantages of the Invention]

[0015]

According to the present invention, in the semiconductor memory card which manages data stored therein according to the file system and the access device which accesses the semiconductor memory card, high-rate accessing to the semiconductor memory card can be realized by holding information on access performance of the semiconductor memory card in the semiconductor memory card and by optimizing processes in either side of the access device or semiconductor memory card, or both of them on the basis of

the information.

[Best mode for carrying out the Invention]

[0016]

Hereinafter, a semiconductor memory card and an access device and an access method in accordance with the present invention will be described with referring to figures.

[0017]

(First Embodiment)

Figure 1 is a diagram showing how a semiconductor memory card and an access device of the present invention is to be carried into effect. In Fig. 1, a semiconductor memory card 111 includes a host interface 112 (described as "I/F" in the diagram), CPU 113, RAM 114, ROM 115, a memory controller 116, a nonvolatile memory 117, a first memory 118, and a second memory 119. The host interface 112 is an interface for transmitting/receiving a control signal and data to/from an access device 100. The ROM 115 stores a program for controlling the semiconductor memory card 111 therein, and the program uses the RAM 114 as a temporary storage area and operates on the CPU 113. The memory controller 116 is a device for controlling the nonvolatile memory 117 as the data storage area in the semiconductor memory card 111. The memory controller 116 includes a logical-to-physical conversion control section 120, a free

physical area generating section 121, an address management information update control section 122, and a nonvolatile memory access section 123. The details thereof will be given in the descriptions of Second and the following embodiments. The nonvolatile memory 117 includes an address management information 126 and a user data 127. The address management information 126 is a table which administrates correspondence between a physical address in the nonvolatile memory 117 and a logical address which the access device 100 uses for access. The user data 127 is data recorded in the semiconductor memory card 111 by the user. The first memory 118 is an updatable nonvolatile memory, which includes a card information storage section 124 for storing information on access performance of the semiconductor memory card 111. The second memory 119 is an updatable nonvolatile memory and includes a host information storage part 125 for storing information on the access device 100 which accesses the semiconductor memory card 111. The details thereof will be given in the descriptions of Second and the following embodiments.

[0018]

On the other hand, in Fig. 1, the access device 100 which accesses the semiconductor memory card 111 includes CPU 101, RAM 102, ROM 104, and a slot 103. The ROM 104 stores a program for controlling the access device 100

therein, and the program uses the RAM 102 as a temporary storage area and operates on the CPU 101. The slot 103 is a connector between the semiconductor memory card 111 and the access device 100. A control signal and data are transmitted and received between the access device 100 and the semiconductor memory card 111 through the slot 103. Further, the ROM 104 includes an application program 105, a file system controller 106, an access condition determination part 107, a card information acquisition part 108, an access controller 109, and a condition storage part 110 for storing card use condition. The details thereof will be given in the descriptions of Second and the following embodiments.

[0019]

Subsequently, characteristics of a semiconductor memory used as a data recording device in the semiconductor memory card 111 will be described. The semiconductor memory allows formation of a compact, lightweight information recording medium and is thus now establishing itself as a leader of information recording media in various technical fields. The semiconductor memory uses a nonvolatile memory called EEPROM or flash ROM (hereinafter referred to as Flash memory) as a device for information recording. An NAND memory used in a lot of information recording media has characteristic that recorded data in

the medium must be erased once prior to writing of data to return to an unrecorded state and then the data must be written.

[0020]

Here, a data erase unit is referred to as an erase block and managed as a block consisting of a plurality of sectors which are minimum unit of access. Fig. 2 is a view showing an example of the relationship between the erase block and sector in Flash memory. In the example shown in Fig. 2, a single erase block consists of 32 sectors. Access can be performed in units of sectors (512 bytes, for example), while data erasing process necessary before writing is performed in erase block unit (16 KB).

[0021]

Examples of data erasing process and writing process in the semiconductor memory card 111 will be described referring to Figs. 3 and 4. Fig. 3 shows procedural steps in the semiconductor memory card 111 in the case where data having a length of multiples of the erase block is written as an example of the writing process. Fig. 4 shows procedural steps in the semiconductor memory card 111 in the case where data for 1 sector is written.

[0022]

In data recording process in Fig. 3, first, a command and argument transmitted from the access device 100 are

received through the host interface 112 (S301). Next, the received command is referred to determine whether or not the command is an inrecognizable incorrect command (S302). In the case of an incorrect command, error is informed to the access device 100 and the process finishes (S303). In the case of a recognizable command, determination is made whether or not the command is a writing command (S304). In the case of a command other than the writing command, the other process corresponding to each command is performed (S305). In the case of the writing command, a physical address of the erase block at which data is actually written in the Flash memory is determined from information on a writing position and writing size stored in the argument (S306). Next, prior to writing, data existing in the erase block in the Flash memory, which is determined in the S306, is erased through the memory controller 116 (S307). Next, data for 1 sector is received from the access device 100 through the host interface 112 (S308). When data reception is finished, the received data for 1 sector is written to the Flash memory through the memory controller 116 (S309). The data reception and writing process in S308 and S309 is repeatedly performed until writing of the data for 1 erase block is finished (S310). The data writing process for 1 erase block from S306 to S310 is repeatedly performed until the data writing

designated from the access device 100 is finished (S311). When the data writing for the writing size designated from the access device 100 is finished, the operation comes to an end.

[0023]

The data recording process in Fig. 4 is different from the process in Fig. 3 in that data other than the data for 1 sector received from the access device 100 of the data contained in the erase block to be written in S410 is written to the erase block determined in S406. In the NAND type memory, data needs to be erased once prior to data writing and the erasing process can be performed only in erase block unit. Thus, also when data for 1 sector is written, it is necessary to erase data for 1 erase block and, rewrite existing data contained in the same erase block to a new erase block as in the process in S410.

[0024]

As shown in Figs. 3 and 4, the data recording process is roughly divided into three processes: command interpretation process, data erasing process, and data writing process. For example, Flash memory by which command interpretation overhead takes 3 ms, writing process for 1 sector takes 200 μs, and erasing process for 1 erase block (16 KB) takes 2 ms is assumed. When in data writing for 1 erase block (16 KB) to this Flash memory, the process

shown in Fig. 3 is performed, and it takes 3 ms for command interpretation, 2 ms for erasing process, and 32×200 μs for writing process, or 11.4 ms in total. Similarly, when in data writing for 1 sector (512 B), the process shown in Fig. 4 is performed, and it takes 3 ms for command interpretation, 2 ms for erasing process, and 200 μs + 31×200 μs for writing process, or 11.4 ms in total. That is, data writing of 16 KB and data writing of 1 sector data take the same time period. Although the case where there is an extreme difference in performance with disregard to data transfer time, and etc. is described in this example, in the actual Flash memory, writing time becomes minimum when writing is performed in units of erase blocks.

[0025]

Moreover, in the semiconductor memory card 111, a plurality of Flash memories may be used as recording devices. Fig. 5 is a view showing an example of the configuration of the semiconductor memory card 111 in which two Flash memories are used. In each of the two Flash memories shown in Fig. 5, a single erase block consists of 32 sectors, and physical sector numbers in ascending order are given to each sector existing in the two Flash memories so that the two Flash memories may be alternatively replaced in units of 32 sectors. In the case of the semiconductor memory card 111 composed of a plurality of

Flash memories, by designing it so that reading-writing process can be performed in parallel with respect to a plurality of Flash memories, high-rate access can be achieved. For example, in the example shown in Fig. 5, when data is written in 64 sectors having the physical sector numbers 0 to PSN 63, data can be written at high-rate by writing the data to the two erase blocks 0_0 and 1_0 in parallel.

[0026]

Figure 6 shows timing of writing data of 1 erase block size and timing of writing data of 2 erase blocks size in the case where the semiconductor memory card 111 is composed of two Flash memories shown in Fig. 5. In Fig. 6, T1 represents required time for writing process of 1 erase block. T1' + T2' represents required time for parallel writing process of two erase blocks. That is, writing process time in the case where data is written in one by one erase block in two writings becomes T1×2 and writing process time in the case where data is written to two erase blocks in parallel becomes the T1' + T2'. The T1' is required time for the process without writing to the Flash memories and is very short. The T2' is required time for parallel writing process to the two Flash memories and is slightly longer than the time T1 required for writing process to one Flash memory, and however, does not reach

time twice as much as T1. For this reason, in the example shown in Fig. 6, writing time becomes shortest when data is written to the semiconductor memory card 111 in units of two erase blocks. In other words, writing time to the semiconductor memory card 111 depends on the number of Flash memories used in the semiconductor memory card 111 and management method of the Flash memory as well as the size of the erase block. Furthermore, access performance of the semiconductor memory card 111 varies depending on differences in generation and manufacturer of the semiconductor memory card 111. Thus, in this embodiment, information on access performance which varies from semiconductor memory card 111 to the memory card 111 is held in the memory card 111 so as to be acquired by the access device 100. Whereby, the access device 100 becomes able to recognize an optimum access method for each semiconductor memory card 111 so that high-rate access to the semiconductor memory card 111 can be realized.

[0027]

Subsequently, a card information storage part 124 in this embodiment will be described. The card information storage part 124 is a section for storing information on access performance of the semiconductor memory card 111 therein. Fig. 7 is a view showing an example of information stored in the card information storage part 124.

Each item by information type will be described below.

[0028]

The first information contained in card information is information on internal physical characteristics of the semiconductor memory card 111. The information includes, for example, the type and number of Flash memory used in the semiconductor memory card 111, management method of the semiconductor memory such as presence or absence of parallel writing to the memory, erase block size of the Flash memory, management block size in the semiconductor memory card 111, temperature conditions, power consumption, current value, voltage value, and card type information for discriminating the type of the card such as a version of standard to which the semiconductor memory card 111 conforms and command set which the semiconductor memory card 111 supports. Such information includes information which serves as a basis for determining the access performance of the semiconductor memory card 111, for example, the number of Flash memories which affects improvement in efficiency of parallel writing process and erase block size which affects optimum process unit size for the semiconductor memory card 111.

[0029]

The second information contained in the card information is information on access conditions to be

fulfilled when the access device 100 accesses the semiconductor memory card 111. The information includes process type, process unit size, process unit boundary, process unit time, access method, minimum sequential area size at sequential access, input clock frequency, and bit width. The process type represents types of process to the semiconductor memory card 111, and there are reading process, writing process, and erasing process and etc. The writing process refers to the following two types of process: writing process including erasing process which becomes necessary when data is overwritten at a position where data has been already written; and process of only writing data at a position where no data exists. The process unit size is the size of one process to the semiconductor memory card 111. The process unit boundary is information representing a process starting position. As described above, the optimum process unit size and process unit boundary for the semiconductor memory card 111 depend on the number of Flash memories processed in parallel in the semiconductor memory card 111, management method, erase block size and etc. That is, in the case where the Flash memories are not processed in parallel in the semiconductor memory card 111, the erase block size of the flash memory is the same as the process unit size. When the process unit boundary is the same as these sizes

at this time, the semiconductor memory card 111 can be efficiently accessed. In the case where a plurality of flash memories are processed in parallel, efficient access can be realized when the process unit size and process unit boundary are the same as the management block size of parallel processing. Furthermore, in the case where the optimum process unit boundary for the semiconductor memory card 111 has the length of multiples of the process unit size, it is possible to omit the process unit boundary and determine the boundary using the process unit size. A process unit time is information representing unit time which serves as a measurement reference of performance value in expressing access performance. The access method represents address designating condition at the time when the access device 100 accesses the semiconductor memory card 111, and there are sequential access of accessing a continuous area, random access of accessing a discontinuous area, and etc. In the semiconductor memory card 111 in which the Flash memories are processed in parallel, even when process is not performed in units of management block sizes to be processed in parallel, but performed by dividing it into smaller units such as erase block units, if process is sequentially performed to continuous areas, process at a certain level of high-rate can be realized depending on the management method of the Flash memories.

Thus, the minimum continuous area size at sequential access represents the size of a minimum continuous area necessary for high-rate access at sequential access. The input clock frequency is information representing basic clock frequency in transmission/reception of a command and data between the access device 100 and semiconductor memory card 111. The bit width is information representing the number of bits of a signal line used for data transfer between the access device 100 and semiconductor memory card 111.

[0030]

The third information contained in the card information is information on the access performance per se of the semiconductor memory card 111. The information includes a flag representing the level of rate performance of the semiconductor memory card 111, data size to be processed within unit time, required time for processing per unit size, transfer rate, and process time inside card of the semiconductor memory card 111. These pieces of information represent the access performance of the semiconductor memory card 111 and vary only in expressing method. Furthermore, the information on the access performance closely relates to the above-mentioned first information and second information. For example, when the input clock frequency is low, the transfer rate of data inputted/outputted from/to the semiconductor memory card

becomes lower, which results in deterioration of the access performance of the semiconductor memory card 111. When the process unit size for accessing the semiconductor memory card 111 is small, the access performance of the semiconductor memory card 111 will be impaired for reason such as that access in erase block unit cannot be performed or the effect of parallel processing cannot be obtained. As described above, the information on the access performance to be stored as the third information is associated with the first information and second information.

[0031]

The Fourth information contained in the card information is information on abnormal process of the semiconductor memory card 111. The information includes error occurrence probability in each of reading process, writing process, and etc., and worst value of time from when the access device 100 issues a command to the semiconductor memory card 111 until the access device 100 receives an error notice. These pieces of information are used when the access device 100 estimates buffer size necessary for the abnormal process.

[0032]

The fifth information contained in the card information is other information on the access performance

of the semiconductor memory card 111. The information includes rate performance level determination reference, rate performance level, and electrical power consumption level. The details of the information will be described later.

[0033]

Figure 7 shows the above-mentioned 5 types of information as information which can be stored in the card information storage part 124. The card information storage part 124 may store all of the information therein, or may select and store therein information necessary for optimum access between the access device 100 and semiconductor memory card 111.

[0034]

The main point in the present embodiment is that information on the access performance of the semiconductor memory card 111 as shown in Fig. 7 is held within the semiconductor memory card 111 and a part or all of the information can be acquired by the access device 100 so as to optimally access the semiconductor memory card 111 from the access device 100. Hereinafter, several methods by which the access device 100 finds the access performance of the semiconductor memory card 111 to realize optimum access to the semiconductor memory card 111 will be described below.

[0035]

As the first method, a method by which the semiconductor memory card 111 returns information on access conditions and access performance values for optimally accessing the semiconductor memory card 111 in response to a request from the access device 100 will be described referring to Figs. 8, 9, and 10.

[0036]

Figures 8 and 9 are views showing procedural steps at the side of the access device 100 in this method and procedural steps at the side of the semiconductor memory card 111 in this method, respectively. Fig. 10 is a view showing an example of access conditions and access performance values that the semiconductor memory card 111 eventually returns to the access device 100.

[0037]

At first, the procedural steps at the side of the access device 100 will be described referring to Fig. 8. In this process shown in Fig. 8, the access device 100 firstly issues a command (card type acquisition command) to the semiconductor memory card 111 to acquire card type information, such as a version of standard to which the semiconductor memory card 111 conforms, of the semiconductor memory card 111 (S801). Next, it is determined whether or not the card type information is

acquired from the semiconductor memory card 111 according to the issued command (S802). When acquisition is unsuccessful, it is determined that an error has occurred and the operation comes to an end (S803). When acquisition is successful, based on the acquired information, it is determined whether or not the semiconductor memory card 111 responds to a command (optimum access information acquisition command) to acquire access conditions for optimally accessing the semiconductor memory card 111 and access performance values at this time from the semiconductor memory card 111 (S804). When the semiconductor memory card 111 does not responds to the command, acquisition of the access conditions and access performance values is canceled and the operation comes to an end (S805). When the semiconductor memory card 111 responds to the command, the optimum access information acquisition command is issued to the semiconductor memory card 111 (S806). Next, it is determined whether or not the access conditions and access performance values have been acquired from the semiconductor memory card 111 according to the issued command (S807). When acquisition is unsuccessful, it is determined that an error has occurred and the operation comes to an end (S808). When acquisition is successful, the operation is normally finished.

[0038]

Subsequently, the procedural steps at the side of the semiconductor memory card 111 will be described referring to Fig. 9. Fig. 9(a) is a view showing process at the side of the semiconductor memory card 111 when the card type acquisition command is issued from the access device 100 as described with reference to Fig. 8. Fig. 9(b) is a view showing process at the side of the semiconductor memory card 111 when the optimum access information acquisition command is issued from the access device 100 as described with reference to Fig. 8. In the process at the side of the semiconductor memory card 111 as shown in Fig. 9(a), the semiconductor memory card 111 firstly receives a command from the access device 100 (S901). Next, referring to the received command, it is determined whether or not the command is an unrecognizable incorrect command (S902). When the received command is an incorrect command, an error is informed to the access device 100 and the operation comes to an end (S903). When it is a recognizable command, it is determined whether or not the command is the card type acquisition command (S904). When the received command is a command other than the card type acquisition command, other process responding to each command is performed (S905). When the command is the card type acquisition command, the card type information stored in the card information storage part 124 is read from the card

information storage part 132 (S906). Lastly, the card type information thereby read is transmitted to the access device 100 and the operation comes to an end (S907). Likewise, in the process as shown in Fig. 9(b), process corresponding to the optimum access information acquisition command issued from the access device 100 is executed. The process shown in Fig. 9(a) is different from that shown in Fig. 9(b) in that it is confirmed whether or not a received command is the optimum access information acquisition command at Step S911, and that, when the command is the optimum access information acquisition command, the access conditions for optimally accessing the semiconductor memory card 111 and the corresponding access performance values are read from the card information storage part 124 at Step S913, and also that the thereby read access conditions and access performance values are transmitted to the access device 100 at Step S914.

[0039]

In this way, according to the procedural steps shown in Figs. 8 and 9, the access device 100 can acquire the access conditions for optimally accessing the semiconductor memory card 111 and the corresponding access performance values from the semiconductor memory card 111. Fig. 10 is a view showing an example of the access conditions and access values. As shown in Fig. 10(a), the access

condition shows information on conditions to be fulfilled by the access device 100 to optimally access the semiconductor memory card 111, such as process unit size, process unit boundary, access method, input clock frequency, and bit width. Moreover, as shown in Fig. 10(b), the access performance value is information showing processing performance in the case where the access device 100 performs access according to the above-mentioned access conditions, such as a mean value and a worst value of transfer rate in each of reading process, writing process, and erasing process. By acquiring these pieces of information from the semiconductor memory card 111, the access device 100 becomes able to recognize how optimum access to the semiconductor memory card 111 should be made and how much access performance is obtained in this case. Thus, optimum access according to characteristics of the semiconductor memory card 111 can be realized.

[0040]

Subsequently, as the second method, a method by which the access device 100 inputs the access conditions in the semiconductor memory card 111 and the semiconductor memory card 111 returns the access performance values will be described referring to Figs. 11, 12, and 13.

[0041]

Figures 11 and 12 are views showing procedural steps

at the side of the access device 100 in this method and procedural steps at the side the semiconductor memory card 111 in this method, respectively. Fig. 13 is a view showing an example of the access conditions that the access device 100 inputs in the semiconductor memory card 111 and the access performance values that the semiconductor memory card 111 returns to the access device 100.

[0042]

The process at the side of the access device 100 as shown in Fig. 11 is different from the first method in that the optimum access information acquisition command is replaced with an access performance value acquisition command. In this method, since the access device 100 inputs the access conditions to the semiconductor memory card 111, the access performance value acquisition command is a command having the access conditions as arguments.

[0043]

Next, the procedural steps at the side of the semiconductor memory card 111 will be described referring to Fig. 12. In this method, like the first method, the card type acquisition command is issued from the access device 100, and the process at the side of the semiconductor memory card 111 is the same as that shown in Fig. 9(a). Fig. 12 is a view showing the process at the side of the semiconductor memory card 111 in the case where

the access performance value acquisition command is issued from the access device 100 as described with reference to Fig. 11. In the process shown in Fig. 12, the steps ranging from S1201 to S1205 are the same as those in the process shown in Fig. 9(b), the description thereof will be omitted. By the procedural steps thus far described, the semiconductor memory card 111 recognizes that the access performance value acquisition command has been issued from the access device 100. After that, the semiconductor memory card 111 reads the access conditions and access performance values from the card information storage part 124 (S1206). Next, referring to the read access conditions and corresponding access performance values, it is determined whether an access performance value matching with the access condition which the access device 100 designates in the command arguments exist or not (S1207). When the access performance value does not exist, an error is informed to the access device 100 and the operation comes to an end (S1209). When the access performance value exist, the access performance value of interest is transmitted to the access device 100 and the operation comes to an end (S1210).

[0044]

As described above, in the procedure described in Figs. 11 and 12, the access device 100 can input the access

conditions to the semiconductor memory card 111 and acquire the access performance values according to the conditions. Fig. 13 is a view showing an example of the access conditions and the access performance values. As shown in Fig. 13 (a), the access conditions that the access device 100 inputs to the semiconductor memory card 111 are information representing conditions to be fulfilled when making access to the semiconductor memory card 111, for example, process unit size, process unit boundary, access method, input clock frequency, and bit width. Moreover, the access performance values shown in Fig. 13(b) are the same information as that shown in Fig. 10(b); that is, the access performance values according to the access conditions inputted by the access device 100. In this manner, by inputting the conditions for accessing the semiconductor memory card 111 and acquiring the access performance values according to the conditions from the semiconductor memory card 111, the access device 100 can determine whether or not desired access performance can be obtained according to the assumed access method.

[0045]

Subsequently, as the third method, a method by which the access device 100 inputs the access performance values to the semiconductor memory card 111 and the semiconductor memory card 111 returns the access condition will be

described referring to Figs. 14 and 15.

[0046]

Figures 14 and 15 are views showing procedural steps at the side of the access device 100 in this method and procedural steps at the side of the semiconductor memory card 111 in this method, respectively. The process as shown in Figs. 14 and 15 is different from the second method in that the access performance value acquisition command is replaced with an access condition acquisition command and that information to be inputted to the semiconductor memory card 111 and information to be outputted from the semiconductor memory card 111 change places with each other.

[0047]

By the procedural steps shown in Figs. 14 and 15, the access device 100 can input the access performance values to the semiconductor memory card 111 and acquire the access conditions according to the performance values. The access conditions and access performance values in this method are the same as the information as shown in Fig. 10. In this method, performance values required in accessing to the semiconductor memory card 111 are inputted and the access conditions to which the access device 100 should obey to meet the performance values are acquired from the semiconductor memory card 111. In this manner, the access

device 100 becomes able to recognize how to access the semiconductor memory card 111 to meet the desired access performance, thereby enabling access with the desired access performance to be realized.

[0048]

Subsequently, as the fourth method, a method by which the access device 100 inputs the access conditions and access performance values to the semiconductor memory card 111 and the semiconductor memory card 111 returns whether or not the input access performance values are met in the case of access on the input access conditions will be described referring to Figs. 16 and 17.

[0049]

Figures 16 and 17 are views showing procedural steps at the side of the access device 100 in this method and procedural steps at the side of the semiconductor memory card 111 in this method, respectively. The process as shown in Fig. 16 is different from the first method in that the optimum access information acquisition command is replaced with an optimum access propriety determination command. In this method, since the access device 100 inputs the access conditions and access performance values to the semiconductor memory card 111, the optimum access propriety determination command is a command having the access conditions and access performance values as

arguments. Moreover, information acquired from the semiconductor memory card 111 as the result of the command becomes the determination result of whether the designated access performance values are met in the case of access on the designated access conditions.

[0050]

Next, the procedural steps at the side of the semiconductor memory card 111 will be described referring to Fig. 17. In this method, like the first method, the card type acquisition command is issued from the access device 100, and the process at the side of the semiconductor memory card 111 is the same as that shown in Fig. 9(a). Fig. 17 is a view showing the process at the side of the semiconductor memory card 111 in the case where the optimum access propriety determination command is issued from the access device 100 as described with reference to Fig. 16. In the process shown in Fig. 17, the steps ranging from S1701 to S1705 are the same as those in the process shown in Fig. 9(b), the description thereof will be omitted. By the procedural steps thus far described, the semiconductor memory card 111 recognizes that the optimum access propriety determination command has been issued from the access device 100. After that, the semiconductor memory card 111 reads the access conditions and access performance values from the card information

storage part 124 (S1706). Next, referring to the thereby read access conditions and corresponding access performance values, it is determined whether or not the access performance value designated by the access device 100 is met when the access device 100 performs access on the access condition designated in the arguments of the command (S1707). When the access performance value is met, the fact that the access performance value is met is informed to the access device 100 and the operation comes to an end (S1709). When the access performance value is not met, the fact that the access performance value is not met is informed and the operation comes to an end (S1710).

[0051]

As described above, in the procedural steps shown in Figs. 16 and 17, the access device 100 can input the access conditions and access performance values to the semiconductor memory card 111 and confirm whether or not the access performance values are met when accessing the semiconductor memory card 111 on the access conditions. The examples of the access conditions and the access performance values in this method are similar to the information shown in Fig. 13. According to this method, by inputting the access conditions and the access performance values to the semiconductor memory card 111 and confirming whether or not the access performance values are met when

accessing the semiconductor memory card 111 on the access conditions, prior to access, the access device 100 becomes able to recognize whether or not desired access performance is met in the assumed access method.

[0052]

Subsequently, as the fifth method, a method whereby a flag representing rate performance level of the semiconductor memory card 111 is used in place of the access performance value described in the first to fourth methods or is contained in the access performance value will be described referring to Fig. 18. The process between the access device 100 and semiconductor memory card 111 in this method corresponds to any of the processes described in the first to fourth methods.

[0053]

Figure 18 is a view showing an example of rate performance level determination criteria in this method and an example of determination results. The rate performance level determination criteria shown in Fig. 18 adopts, as values used for determination, average values of transfer rate in each of reading process, writing process and erasing process, and, based on the determination criteria, one of the rate performance levels: "high-rate, "medium-rate", and "low-rate" is allocated to each access performance value. Similarly, as to the worst values of

transfer rate, rate performance level determination criteria exist. As a result, in the example shown in Fig. 18(b), the rate performance level "high-rate" is allocated to each access performance value. The rate performance level determination criteria shown in Fig. 18(a) are stored in the card information storage part 124.

[0054]

In this method, the access performance of the semiconductor memory card 111 is classified not only in numerical value but in objective level in this manner so that the access device 100 can acquire level from the semiconductor memory card 111. Thus, the access device 100 can easily recognize the access performance of the semiconductor memory card 111.

[0055]

Subsequently, as the sixth method, a method whereby the access device 100 inputs a flag representing power consumption level of the semiconductor memory card 111 to the semiconductor memory card 111 according to the first to fourth methods will be described referring to Fig. 19. In this method, the process between the access device 100 and semiconductor memory card 111 corresponds to any of the processes described in the first to fourth methods. Here, the case where the process is applied to the first method is described as an example. The process at the side of the

access device 100 in this method is similar to the procedural steps shown in Fig. 8. However, a distinction between them lies in that the power consumption level representing the level of power consumption is added as an argument of the optimum access information acquisition command issued to the semiconductor memory card 111 by the access device 100. The power consumption level refers to the degree of the power consumed by the semiconductor memory card 111, and it is represented by a plurality of levels. For example, the power consumption is represented in 3 grades of "large power consumption", "medium power consumption" and "small power consumption".

[0056]

Next, the procedural steps at the side of the semiconductor memory card 111 as shown in Fig. 19 will be described. The points of difference from the first method are that, at Step S1906, it is determined whether the power consumption level designated as the argument of the optimum access information acquisition command issued from the access device 100 is a valid value or not, and, at Step S1908, the access conditions and access performance values for optimum access in the designated power consumption level are read from the card information storage part 124. That is, in this method, it is assumed that there are present plural pieces of information stored in the card

information storage part 124 in a state of being associated with the power consumption level, and information according to the power consumption level designated by the access device 100 is selected and the selected information is transmitted to the access device 100.

[0057]

In this method, when information on access performance is thus acquired from the semiconductor memory card 111, a value representing the power consumption level that the access device 100 assumes is designated in the semiconductor memory card 111, and the access device 100 acquires information on access performance observed at the time when the semiconductor memory card 111 operates with the designated electrical power consumption. Whereby, for example, when the access device 100 intends to drive the semiconductor memory card 111 with low power consumption, the access device 100 becomes able to recognize necessary access conditions and corresponding access performance values.

[0058]

Subsequently, as the seventh method, a method by which the semiconductor memory card 111 returns information that the access device 100 minimally requires to calculate the access performance values will be described referring to Figs. 20 to 24.

[0059]

Figures 20 and 21 are views showing procedural steps at the side of the access device 100 in this method and procedural steps at the side of the semiconductor memory card 111 in this method, respectively. Fig. 22 is a view showing an example of the access performance basic information list that the semiconductor memory card 111 returns to the access device 100. Figs. 23 and 24 are views each showing an example of timing of command-response between the access device 100 and semiconductor memory card 111.

[0060]

The process at the side of the access device 100 as shown in Fig. 20 is different from the first method in that the optimum access information acquisition command is replaced with an access performance basic information list acquisition command, that access performance values are calculated on the basis of the access performance basic information list at Step S2009, and that access conditions required to meet the access performance necessary for the access device 100 are calculated on the basis of the calculated access performance values at Step S2010. These two steps will be described with reference to Figs. 22, 23, and 24 following the explanation of the procedural steps at the side of the semiconductor memory card 111 in this

method.

[0061]

Next, the procedural steps at the side of the semiconductor memory card 111 as shown in Fig. 21 will be described. In this method, like the first method, the card type acquisition command is issued from the access device 100, and the process at the side of the semiconductor memory card 111 is the same as that shown in Fig. 9(a). Fig. 21 is a view showing the process at the side of the semiconductor memory card 111 in the case where the access performance basic information list acquisition command is issued from the access device 100 as described with reference to Fig. 20. The process shown in Fig. 21 is different from the process shown in Fig. 9(b) in that, instead of the access conditions and access performance values, the access performance basic information list is read from the card information storage part 124. The detailed description of this process will be omitted.

[0062]

Next, with reference to Figs. 22, 23, and 24, the access performance basic information list and a method of calculating access performance values using this list will be described. Numerical values representing the access performance of the semiconductor memory card 111 include transfer rate, for example. However, since factors for

determining the transfer rate between the access device 100 and semiconductor memory card 111 exist not only in the semiconductor memory card 111 but also in the access device 100, the conditions set for the access device 100 need to be considered to derive actual transfer rates. In this method, by allowing the access device 100 to acquire information on determination factors of the access performance at the side of the semiconductor memory card 111, the access device 100 can calculate the access performance in consideration of the factors at the side of the access device 100.

[0063]

Figure 22 is a view showing an example of the access performance basic information list which is information on the factors for determining the access performance at the side of the semiconductor memory card 111. As the factor, internal card processing time is used. Next, a method of calculating access performance values on the basis of the access performance basic information list shown in Fig. 22 will be described. Figs. 23 and 24 are views showing an example of timing of command-response between the access device 100 and semiconductor memory card 111. Figs. 23(a), 23(b), and 24 correspond to reading process, writing process, and erasing process, respectively. The access performance value in the reading process shown in Fig.

23(a) is calculated on the basis of a total of command issuance processing time RT1, internal card processing time RT2, and data transfer time RT3. Here, the RT1 and RT3 are time periods determined depending on a clock frequency which is inputted to the semiconductor memory card 111 by the access device 100 and the time can be calculated at the side of the access device 100. On the other hand, the RT2 is a time period required for internal card processing and is determined depending on the semiconductor memory card 111. Thus, the access performance basic information list acquired from the semiconductor memory card 111 stores information necessary for determining the RT2 therein. Similarly, the access performance value in the writing process shown in Fig. 23(b) is calculated on the basis of a total of command issuance processing time WT1, internal card processing time WT2, and data transfer time WT3. Therefore, just as with the reading process, the access performance basic information list stores information necessary for determining the WT2 therein. Similarly, the access performance value in the erasing process shown in Fig. 24 is calculated on the basis of a total of command issuance process time ET1 and internal card processing time ET2. Therefore, just as with the reading process, the access performance basic information list stores information necessary for determining the ET2 therein.

[0064]

Here, with the writing process taken up as an example, an example of access performance value calculation will be described. Time required for data processing of unit size (whole write time: WT_A) is calculated as the access performance value. WT_A can be obtained according to the following equation (1): $WT\_A = WT1 + \sum WT2 + \sum WT3$.

[0065]

Here, assuming that the data transfer amount required from command input until response acquisition is completed is 160 bits and the input clock frequency is sMHz, then the command issuance processing time WT1 can be obtained according to the following equation (2): $WT1 = 160 / (s \times POW(10, 6))$.

[0066]

Here, POW (X, Y) means X raised to the Y^{th} power. Next, $\sum WT2$ represents the sum total of time required for internal card processing can be obtained according to the following equation (3): $\sum WT2 = t \times n / 512$ when it is assumed that the busy time described in Fig. 22(b) is t (second) and the process unit size is n (byte).

[0067]

Next, $\sum WT3$ represents the sum total of data transfer time and can be obtained according to the following equation (4): $\sum WT3 = (1049 \times n / 512) / (s \times POW (10, 6))$

when it is assumed that 4 bits is used as the bit width and that the total number of transfer clocks is 1049 clocks in the case where CRC which is added to confirm validity of the transfer data is added to data of 512 bytes.

[0068]

Therefore, assuming that the input clock frequency is 25 MHz, that the process unit size is 128 KB, and that the access method is sequential access as an example of calculation, then t becomes 9.2 μs and WT_A is calculated as 13.1 ms.

[0069]

In this method, information on factors for determining the access performance at the side of the semiconductor memory card 111 is acquired from the access device 100. Thus, the access device 100 can calculate the access performance in consideration of the factors at the side of the access device 100.

[0070]

Next, as the eighth method, a method by which the semiconductor memory card 111 returns a list of access performance values under various access conditions at a request of the access device 100 will be described referring to Figs. 25 to 29.

[0071]

Figures 25 and 26 are views showing the procedural

steps at the side of the access device 100 in this method and the procedural steps at the side of the semiconductor memory card 111 in this method, respectively. Figs. 27, 28, and 29 are views each showing an example of an access performance table that the semiconductor memory card 111 returns to the access device 100.

[0072]

The process at the side of the access device 100 as shown in Fig. 25 is different from the seventh method in that the access performance basic information list acquisition command is replaced with an access performance table acquisition command, and that access performance value calculation is not carried out. The detailed description of this process will be omitted. Moreover, the process at the side of the semiconductor memory card 111 as shown in Fig. 26 is different from the seventh method in that the access performance basic information list is replaced with an access performance table. The detailed description of this process will be omitted. That is, this method is different from the seventh method in that, since the access device 100 acquires information on access performance per se from the semiconductor memory card 111, there is no need to conduct access performance calculation at the side of the access device 100. Figs. 27, 28, and 29 are views each showing an example of the access performance

table. Fig. 27 shows the size of data which can be processed in unit time. Fig. 28 shows required time for unit size data processing. Fig. 29 shows access performance as processing rate at the time of access in unit size. These pieces of information are different from each other only in their expressing method of access performance and all information expresses the access performance of the semiconductor memory card 111.

[0073]

In this method, the access device 100 can acquire the access performance table and thus recognize a list of the access conditions with respect to the semiconductor memory card 111 and access performance values in accessing the semiconductor memory card under each access condition. Whereby, the access device 100 becomes able to recognize how much the access performance value is in the case of access under the access condition that the access device 100 assumes in itself or on what access condition access should be done to meet the access performance value that the access device 100 requires in itself.

[0074]

As described above, in the semiconductor memory card 111 in accordance with this embodiment, the card information storage part 124 holds therein access performance at the time the access device 100 accesses the

semiconductor memory card 111. The semiconductor memory card 111 transmits a part or all of the information to the access device 100 in response to a request of the access device 100. This allows the access device 100 to know the access performance of the semiconductor memory card 111. Therefore, the access device 100 can access the semiconductor memory card 111 according to an optimum access method, thereby bringing out the best performance of the semiconductor memory card 111.

[0075]

It is noted that the information stored in the card information storage part 124 may be updatable. For example, the rate performance level determination criteria as shown in Fig. 18(a) are inputted from outside of the semiconductor memory card 111 in an updatable manner. In this configuration, the determination criteria can be changed later by performing update. As still another example, when access performance information varies with a change in the internal state of the semiconductor memory card 111, the internal state is monitored in the semiconductor memory card 111. In this configuration, the access performance information may be changed in accordance with the change of the internal state. Furthermore, although determination of the type of the semiconductor memory card 111 is made at the beginning of all processes

at the side of the access device 100 in this embodiment, the type determination may be made only once when accessing the semiconductor memory card 111 for the first time. Furthermore, there is no need to use all of the information on the access performance shown in Fig. 7, and therefore only a part of the information may be used or a part of the information may be used in combination with other information. Moreover, although the example in which the rate performance level and the power consumption level are each represented in three grades is described, they may be represented in a plurality of grades other than the three grades. Furthermore, although three types of examples shown in Fig. 27, Fig. 28, and Fig. 29 are described as the access performance tables, other expression form may be used as long as the information represents the access performance of the semiconductor memory card 111, and also a plurality of expression forms may be used in combination. Moreover, although the first memory 118 which stores the card information therein is described as an updatable nonvolatile memory, an unupdatable nonvolatile memory such as ROM may be used when the memory need not be updated. In addition, the card information may be stored in the nonvolatile memory 117 instead of the first memory 118.

[0076]

(Second embodiment)

By way of the second embodiment of the present invention, a method of acquiring information on the access performance of the semiconductor memory card from the semiconductor memory card having the card information storage part and using the information for file system control the access device will be described.

[0077]

The configuration of the semiconductor memory card and access device in accordance with this embodiment is the same as the configuration shown in Fig. 1. In this embodiment, especially, a file system controller 106, an access condition determination part 107, a card information acquisition part 108, and a card use condition storage part 110 present in the access device 100 will be described in detail.

[0078]

Prior to the detailed description of this embodiment, a FAT file system will be described as an example of a file system used for managing data stored in the semiconductor memory card 111. Fig. 30 shows the configuration of the FAT file system. A file system management area shown in Fig. 30 means an area to be managed according to the file system of the nonvolatile memory 117 within the semiconductor memory card 111 and corresponds to whole or a part of the area described as "user data" 127 in Fig. 1.

In the FAT file system, a management information area 3001 for managing the whole of the file system management area exists at the head of the file system management area, followed by a data area 3002 for storing data and the like held in the file. The management information area 3001 consists of a master boot record and partition table 3003, a partition boot sector 3004, FAT 3005, FAT 3006, and a route directory entry 3007.

[0079]

The master boot record and partition table 3003 is a part which stores therein information for managing the file system management area by dividing it into a plurality of areas called partitions. The partition boot sector 3004 is a part which stores management information in 1 partition therein. The FAT 3005 and the FAT 3006 are parts which represent physical storage positions of data contained in a file. The route directory entry 3007 is a part which stores therein information on a file and directory existing immediately below a route directory. Moreover, the FAT 3005 and the FAT 3006 are important areas representing physical storage positions of the data contained in the file. Accordingly, two pieces of FAT 3005 and 3006 having the same information generally exist in the file system management area for duplication.

[0080]

The data area 3002 is managed by being divided into a plurality of clusters, and data contained in the file is stored in each cluster. A file which stores a lot of data therein stores the data over a plurality of clusters, and the link between the clusters is managed by link information stored in the FAT 3005, 3006. Now, an example of data storage in the FAT file system will be described referring to Fig. 31. The data area 3002 is managed in units of fixed length blocks called clusters and cluster numbers starting from 2 in ascending order are given to each cluster. The FAT 3005, 3006 manages link information representing the use state of each cluster and the link between the clusters, and consists of FAT entries corresponding to the cluster numbers. The FAT entry has any size of three types of 12 bit, 16 bit, and 32 bit per cluster according to the type of the FAT file system. In the example shown in Fig. 31, the case where 1 entry is represented by 16 bits is shown. Any value of the cluster number of a next linked cluster, 0x0000 representing that the concerned cluster is the free area, and 0xFFFF representing that the concerned cluster is a link termination is stored in the FAT entry. In the example shown in Fig. 31, the FAT entries corresponding to the cluster numbers 2, 5, and 7 store 0x0000 therein, which indicates that the three clusters are free areas. Moreover,

the FAT entry corresponding to the cluster number 3, the FAT entry corresponding to the cluster number 4, and the FAT entry corresponding to the cluster number 6 store 0x0004, 0x0006, and 0xFFFF, respectively, which indicates that data is divided and the divided data are stored in the three clusters corresponding to the cluster numbers 3, 4, and 6, respectively.

[0081]

Next, an example of a file data writing in the FAT file system will be described referring to Figs. 32, 33, and 34. Fig. 32 is a view showing file data writing process steps in the FAT file system. Figs. 33 and 34 show an example of a directory entry 3301, the FAT 3005, 3006, and the data area 3002 before and after the writing process, respectively. In the FAT file system, the directory entry 3301 which stores information such as file name, file size, and file attribute therein is stored in a part of the route directory entry 3007 and data area 3002. Fig. 33(a) shows an example of the directory entry 3301. A file indicated by the directory entry 3301 has a file name of FILE1. TXT and stores data in the file therein starting from the cluster number 10. Moreover, the file size is 16000 bytes. In Fig. 33, the size of 1 cluster is assumed to be 4096 bytes and the file data is stored over four clusters.

[0082]

Now, file data writing process will be described referring to Fig. 32. In this process, firstly, the directory entry 3301 of a target file is read (S3201). Next, a file starting cluster number stored in the read directory entry 3301 is acquired to confirm a starting position of file data (S3202). Next, the FAT 3005 and the FAT 3006 are read and a link is tracked on the FAT 3005, 3006 from the starting position of the file data acquired at S3202 to acquire a cluster number at a writing position (S3203). Next, it is determined whether or not a free area needs to be newly allocated to the file at the time of data writing (S3204). When allocation of the free area is unnecessary, the operation proceeds to the process at S3206. When allocation of the free area is necessary, a free area search is performed on the FAT 3005, 3006 and the free area of 1 cluster is allocated to the termination of the file (S3205). Next, data to be written on the cluster referred currently is written to the data area 3002 as much as possible (S3206). Next, it is determined whether or not writing of all data is finished (S3207). When some data still remains, the operation returns to the process at S3204. When writing of all data is finished, the file size and time stamp stored in the directory entry 3301 is updated and written to the semiconductor memory card 111 (S3208). Lastly, the FAT 3005, 3006 is written to the

semiconductor memory card 111 and the operation comes to an end (S3209).

[0083]

When data of 1000 bytes is further written to the file FILE1. TXT having the data of 16000 bytes shown in Fig. 33 according to the file data writing process, as shown in Fig. 34, the file is changed to a file having data of 17000 bytes.

[0084]

In this manner, in the FAT file system, an area is allocated in units of clusters as a file data storage area and data is stored in the area. Furthermore, a plurality of clusters allocated to a single file are not necessarily continuous, and discontinuous areas may be allocated. In the worst case, the file data is written to the discontinuous areas divided in the units of clusters. In this case, the size of a single access to the semiconductor memory card 111 corresponds to 1 cluster or less. In consequence, when the access unit required to access the semiconductor memory card 111 at the highest rate is larger than the cluster size, access with the best performance of the semiconductor memory card 111 cannot be realized.

[0085]

In this embodiment, by acquiring information on access performance from the semiconductor memory card 111

and using the information for processing of the file system, it is possible to provide the method of accessing the file according to the access method most suitable for the semiconductor memory card 111.

[0086]

Subsequently, file system access unit determination process in this embodiment will be described. The file system access unit (hereinafter referred to as FS access unit) is a management unit newly provided in this embodiment in addition to the cluster generally used as the management unit by which the file system carries out area management. The size of a cluster cannot be easily changed, because its upper limit is defined for ensuring compatibility between devices using the file system. However, the access unit required for optimum access to the semiconductor memory card 111 does not necessarily have the size within the highest cluster size. Thus, in this embodiment, a FS access unit is provided as a new area management unit in addition to a cluster. The FS access unit is determined based on the information on access performance acquired from the semiconductor memory card 111, and is used for file system processing operation. In this way, access according to the characteristics of the semiconductor memory card 111 can be realized while keeping comparability with the existing file system.

[0087]

Referring to Fig. 35, FS access unit determination process in the present embodiment will be described. Fig. 35 is a view showing an example of procedural steps in which the file system control part 106 acquires the FS access unit from the access condition determination part 107. In Fig. 35, firstly, the file system control part 106 requests acquisition of the FS access unit to the access condition determination part 107 (S3501). Next, the access condition determination part 107 requests acquisition of card information to the card information acquisition part 108 (S3502). Next, using any of the methods described in the first embodiment, the card information acquisition part 108 acquires card information from the semiconductor memory card 111 (S3503). When acquisition of the card information is unsuccessful, the card information acquisition part 108 informs an error to the file system control part 106 via the access condition determination part 107, and the operation comes to an end (S3505). When acquisition is successful, the card information acquisition part 108 transmits the card information to the access condition determination part 107 (S3506). Next, the access condition determination part 107 acquires access conditions at the time the access device 100 accesses the semiconductor memory card 111 and card use conditions as information

including a desired access performance value from the card use condition storage part 110 (S3507). Next, comparison is made between the card information and the card use condition to determine whether the process unit size suitable for the card use condition exists or not (S3508). When no suitable process unit size exists, for example, the case where the semiconductor memory card 111 cannot meet the access performance value presented in the card use conditions, the error is informed to the file system control part 106 and the operation comes to an end (S3510). When the suitable process unit size exists, the FS access unit is determined to be the process unit size and the access condition determination part 107 transmits the FS access unit to the file system control part 106, and the operation comes to an end (S3511).

[0088]

In this manner, in this embodiment, comparison is made between the card information and the card use condition, and the FS access unit is determined to be the most suitable access unit to access the semiconductor memory card 111. For example, the semiconductor memory card 111 which exhibits access performance of 6 MB/s under access in units of 16 KB and exhibits access performance of 10 MB/s under access in units of 128 KB is assumed. Here, when the access device 100 requires the access performance

of 8 MB/s, then the FS access unit is determined to be 128 KB. By accessing the semiconductor memory card 111 in units of FS accesses, the desired access performance can be obtained. Furthermore, as an example of the card use conditions, the access conditions and access performance values as shown in Fig. 13 are given. That is, the access conditions shown in Fig. 13 are of information indicative of conditions on the assumed access method for the semiconductor memory card 111, and the access performance values are the values of access performance obtained when accessing the semiconductor memory card 111 under said conditions. The access device 100 holds such access performance information, thereby enabling determination on whether or not the semiconductor memory card 111 can meet the self-requiring access performance.

[0089]

Furthermore, like the first method given in the description of the first embodiment, the procedural steps shown in Fig. 35 are set for the case where the access device 100 does not input the information on the access conditions and access performance values. When there is a need for the access device 100 to input the access conditions and access performance values just as with the second method given in the description of the first embodiment, a step in which the access condition

determination part acquires the card use condition from the card use condition storage part 110 to inform the condition to the card information acquisition part 108 is added between Step S3501 and Step S3502 in the process shown in Fig. 35.

[0090]

Hereinafter, a description will be given as to several methods using the FS access unit determined in the steps shown in Fig. 35 for file system processing operation.

[0091]

As the first method, a method of formatting the file system in consideration of the FS access unit will be described. Fig. 36 shows a configuration example for the case where the file system is formatted in consideration of the FS access unit. In Fig. 36, MBR·PT represents the master boot record and partition table 3003, PBS represents the partition boot sector 3004, and RDE represents the route directory entry 3007. In this embodiment, the size of the management information area 3001 ranging from the master boot record and partition table 3003 to the route directory entry 3007 is so adjusted as to have a length of multiples of the FS access unit. Whereby, the head of the data area 3002 conforms to the FS access unit boundary and the remaining area of the data area 3002 can be efficiently managed in FS access units. Furthermore, since the FS

access unit is so adjusted as to have a length of multiples of the cluster size, area management in the data area 3002 is performed in FS access units and can be matched with area management in cluster units.

[0092]

Subsequently, as the second method, a method of writing file data in consideration of the FS access unit will be described. Fig. 37 is a view showing file data writing procedural steps in this method. In the file data writing process, firstly, it is determined whether or not remaining writing data length is longer than FS access unit length (S3701). When the writing data length is less than the FS access unit length, the operation proceeds to the process at S3708. When the writing data length is greater than or equal to the FS access unit length, prior to writing to the semiconductor memory card 111, data of the FS access unit length is prepared (S3702). Next, a free area search is performed on the FAT 3005, 3006 for each FS access unit and an area in which the area contained in the FS access unit consists of only free clusters is acquired (S3703). When no free area exists, an error is informed and the operation comes to an end (S3705). When the free area exists, data of the FS access unit length is collectively written on the acquired free area (S3706). Next, it is determined whether the writing of all of the

data is finished or not (S3707). When the writing is not finished, the operation returns to the process at S3701. When the writing is finished, the operation comes to an end. Moreover, when it is determined that the remaining data length is shorter than the FS access unit at S3701, then remaining data of the data length shorter than the FS access unit length is prepared (S3708). Next, just as with Step S3703, an area in which the area contained in the FS access unit consists of only free clusters is acquired (S3709). When no free area exists, an error is informed and the operation comes to an end (S3711). When the free area exists, the remaining data is collectively written on the acquired free area and the operation comes to an end (S3712).

[0093]

In the case of the data arrangement as shown in Fig. 38, according to this method, an area of the FS access unit 2 (area of the cluster numbers ranging from 18 to 25) is selected as the file data writing area. In other words, areas of the FS access unit 0 and FS access unit 1 in which file data or directory information of at least 1 cluster exists are not used for the file data writing area. Therefore, since the continuous area in the FS access unit is ensured for file data having a relatively large file size, high-rate access to the semiconductor memory card 111

in optimum access units can be realized.

[0094]

Subsequently, as the third method, a method of allocating a directory area in consideration of the FS access unit will be described. Fig. 39 is a diagram showing procedural steps of directory area allocation in this method. In the directory area allocation process, firstly, a current search pointer is set for the head of the data area (S3901). Next, it is determined whether the directory area exists or not in the currently referred FS access unit (S3902). When no directory area exists, the operation proceeds to the process at S3905. When the directory area exists, it is determined whether a free cluster exists or not in the currently referred FS access unit (S3903). When no free cluster exists, the operation proceeds to the process at S3905. When the free cluster exists, the free cluster is allocated to the directory area and the operation comes to an end (S3904). When no area is found to be present in the determination of S3902 or S3903, it is determined whether or not confirmation of all of the data area 3002 has been completed (S3905). When confirmation has not been completed, the current search pointer is set for the next FS access unit and the operation returns to the process at S3902 (S3906). Then, when confirmation for the whole area is completed, an area

in which the area contained in the FS access unit consists of only free clusters is acquired from the whole of the data area 3002 (S3907). When the free area exists, a single free cluster contained in the acquired area is allocated to the directory area and the operation comes to an end (S3909). When no free area exists, the free clusters are acquired from the whole of the data area (S3910). When no free area exists, an error is informed and the operation comes to an end (S3912). When the free area exists, the acquired free cluster is allocated to the directory area and the operation comes to an end (S3913). [0095]

In the case of the data arrangement as shown in Fig. 40, according to this method, the allocation of free clusters contained in the FS access unit 1 which is the FS access unit already containing the directory area is effected for directory area allocation. By allocating the directory area in this manner, the directory area is preferentially stored in the same FS access unit, resulting in that the free area of FS access unit length is easy to be generated. Thus, the continuous area for file data can be effectively ensured according to the first method. [0096]

Subsequently, as the fourth method, a method of performing defragmentation in consideration of the FS

access unit will be described. Defragmentation is a process in which file data arranged in distribution in a recording medium are rearranged to be placed in the continuous area thereby to achieve high-rate access to the file data. According to this method, in the defragmentation process, defragmentation in consideration of the FS access unit is performed. Fig. 41 is a view showing an example of data arrangement before the defragmentation process. In this example, file data or directory area is stored in all of the three FS access units. Thus, in the free area acquisition process in FS access units in the first method, free area acquisition cannot be achieved. Here, through the defragmentation process in consideration of the FS access unit, the directory area contained in the FS access unit 2 is moved to the free area in the FS access unit 1 to collect the directory areas in the FS access unit 1. Furthermore, the file data in the FS access unit 2 is moved to the free area in the FS access unit 0 to collect the file data in the FS access unit 0. As a result, data arrangement is changed to a state as shown in Fig. 42 where the FS access unit 2 consists of only free areas. In the free area acquisition in FS access units according to the first method, the acquired free area can be allocated as the free area for file data.

[0097]

That is, according to this method, in the defragmentation process, by collecting the directory areas in the same FS access unit and further collecting the file data smaller than the FS access unit size in the same FS access unit, the free area having a length of multiples of the FS access unit is generated to a maximum extent. Thus, the continuous area for file data can be ensured effectively according to the first method. Furthermore, it is unnecessary to combine all areas used for example for storage of file data in the recording medium into a single continuous area thereby to render the whole free area a single continuous area. By performing the defragmentation process solely for the purpose of generating the free area having a length of multiples of FS access unit, required time for the defragmentation process can be shortened.

[0098]

Subsequently, as the fifth method, a method of acquiring remaining free area length in units of FS access units will be described. Fig. 43 is a diagram showing the procedure for remaining free area length acquisition process in this method. In the remaining free area length acquisition process, firstly, 0 is set as a free FS access unit number (S4301). Next, the current search pointer is set for the head of the data area (S4302). Next, it is

determined whether all the clusters of the currently referred FS access unit are free or not (S4303). When the clusters are all free clusters, 1 is added to the free FS access unit number (S4304). Next, it is determined whether confirmation of all areas is completed or not (S4305). When confirmation is not completed, the current search pointer is set for the next FS access unit and the operation returns to the process at S4303. When confirmation is completed, a numerical value stored in the free FS access unit number is converted into the number of bytes, and the number is informed to the application program 105. Then, the operation comes to an end (S4307).

[0099]

In the remaining free area length acquisition process according to this method, in the case of the data arrangement as shown in Fig. 44 for example, three FS access units in which all of the areas in FS access units are free clusters are determined to be free areas.

[0100]

According to this method, by calculating the number of free areas having the FS access unit length and informing the number to the application program 105, the application program 105 becomes able to recognize the remaining free area length in FS access unit. This makes it possible to recognize, at the time of performing access

which meets access performance required by the access device 100 for each FS access unit, how much remaining data can be written with the access performance.

[0101]

As described above, the access device 100 in accordance with the present embodiment acquires information on access performance from the semiconductor memory card 111, determines an optimum access unit, and uses the access unit in file system processing operation. Thus, the access device 100 becomes able to access the semiconductor memory card 111 according to the optimum access method thereby to derive the best performance of the semiconductor memory card 111.

[0102]

Although the description of the present embodiment deals with the example in which the file system control part 106 and other components are realized by the programs on the ROM 104 of the access device 100, all or part of the functions of the programs may be added to the access device 100 in the form of hardware. For example, as shown in Fig. 45, only the application program 105 may be stored in the ROM 104, and the file system control part 106, the access condition determination part 107, the card information acquisition part 108, the access control part 109, and the card use condition storage part 110 may be configured to be

hardware and added to the access device 100 as a semiconductor memory card control LSI 4501. The configuration shown in Fig. 45 is merely an example, and therefore only part of the functions described in the present embodiment, for example, the function of automatically unifying the following data transfer to the semiconductor memory card 111 in FS access units and transmitting the data, may be configured as hardware by setting the FS access unit to the semiconductor memory card control LSI 4501. Furthermore, although the present embodiment has been described by using the FAT file system as an example of the file system, other file system forms such as UDF may be used as long as the file system performs area management for each management unit size on an individual basis. Moreover, in the file data writing process shown in Fig. 37, when no free area in the FS access unit exists, the writing operation results in an error. However, the free area of data length smaller than or equal to the FS access unit length may be acquired and data may be written on the acquired free area. Further, in the description of the remaining free area length acquisition process shown in Fig. 43, although the example in which the remaining free area length is converted into the number of bytes before being informed is given, the remaining free area length may be converted into the number

of sectors or clusters before being informed as long as the remaining free area length can be correctly recognized.

[0103]

(Third embodiment)

Figure 46 is a diagram showing how the third embodiment of the present invention is to be carried into effect. In Fig. 46, numerical symbol 4601 represents a nonvolatile memory wherein two pieces of nonvolatile memory elements (nonvolatile memory chip A and nonvolatile memory chip B) exist. 4602 represents a memory controller. Other blocks are similar to those shown in Fig. 1. The nonvolatile memory 4601 stores the address management information 126 and the user data 127 therein. Note that the nonvolatile memory chip A and the nonvolatile memory chip B are connected to the memory controller 4602 by independent bidirectional buses, respectively.

[0104]

Figure 47 is an explanatory view showing the logical-to-physical conversion control section 120. The logical-to-physical conversion control section 120 is a table for managing process of conversion from a logical address specified by the access device 100 to a physical address and the state of each physical block. Fig. 47(a) shows a logical-to-physical conversion table for converting a logical sector address to a physical sector address. Fig.

47(b) shows an entry table indicating whether each physical block is valid or invalid, or a defective block. Both of the logical-to-physical conversion table and the entry table are stored in a volatile memory such as RAM. In Fig. 47(a), a first half part (ranging in logical address from 0 to N-1) is a table area corresponding to the nonvolatile memory chip A, whereas a latter half part (ranging in logical address from N to 2N-1) is a table area corresponding to the nonvolatile memory chip B. Similarly, also in Fig. 47(b), a first half part (ranging in physical block address from 0 to M-1) is a table area corresponding to the nonvolatile memory chip A, whereas a latter half part (ranging in physical block address from M to 2M-1) is a table area corresponding to the nonvolatile memory chip B. That is, the nonvolatile memory 4601 has 2N-sector space as logical space, and the nonvolatile memory chip A and the nonvolatile memory chip B are logically continuous with each other.

[0105]

Figure 48 is an explanatory view showing erase blocks arranged in each of the nonvolatile memory chips A and B (the unit for selective erasing). The erase block consists of 32 sectors in total, and the capacity per sector is 528 bytes. Each sector area consists of a data area for writing of so-called user data and a management area for

writing of address management information including a flag or the like which indicates that a corresponding logical address and data stored in the data area are valid or invalid, or a defective block. Note that the logical-to-physical conversion table shown in Fig. 47(a) and the entry table shown in Fig. 47(b) are produced on the RAM within the logical-to-physical conversion control section 120 by reading information stored in the management area of each erase block of the nonvolatile memory chips A and B by the CPU 113 at the time of initialization immediately after power-up.

[0106]

Figure 49 is a flow chart showing process to be conducted in the free physical area generating section 121.

[0107]

Figure 50 is a time chart showing the form of access from the nonvolatile memory access section 123 to the nonvolatile memory 4601.

[0108]

Referring mainly to Figs. 49 and 50, the semiconductor memory card and the access device thereby constructed will be described in respect of their workings. Firstly, the access device 100 transfers, in addition to a writing command, the start sector address SA and writing size L to the semiconductor memory card 111. The start

sector address SA and writing size L are temporarily stored in the host information storage part 125. On the basis of the start sector address SA and writing size L temporarily stored in the host information storage part 125 and a parameter indicative of the boundary of the first half area and the latter half area in the nonvolatile memory 4601 (sector address number: N), the memory controller 4602 determines whether writing is performed on the first half area (semiconductor memory chip A) only, or on the latter half area (semiconductor memory chip B) only, or across the first and latter half areas. In Fig. 49, the left part, the right part, and the middle part of the chart with respect to the main routine correspond to writing to the first half area (semiconductor memory chip A) only, writing to the latter half area (semiconductor memory chip B) only, and writing across the first and latter half areas, respectively. Fig. 50 shows a time chart for the case where writing is performed on the first half area (semiconductor memory chip A) only, with the writing size set at 4 KB. As employed in a sequence for writing to the first half area (semiconductor memory chip A) only, writing command issuance time refers to a period of time over which an instruction for writing to the nonvolatile memory chip A and a writing destination address are transferred, data transfer time refers to a period of time over which writing

data is transferred to the nonvolatile memory chip A, and program busy time refers to a period of time over which the writing data is programmed (written) to the nonvolatile memory chip A. Meanwhile, a sequence for access to the latter half area (nonvolatile memory chip B) consists of erasing command issuance time (erasing instruction to the nonvolatile memory chip B and designation of erasing target block address) and erasing busy time (erasing of erasing target block). In the case where a NAND flash memory or the like is used as the nonvolatile memory, the erasing busy time becomes longer than the program busy time (2 msec, for example). The third embodiment deals with the case where a time period of 2 msec (equivalent to erasing time) is required when the writing size is 4 KB, and the nonvolatile memory access section 123 determines whether or not to erase a nonvolatile memory chip other than a nonvolatile memory chip to be written upon (here, the nonvolatile memory chip B); that is, determines whether or not to issue an erasing command, depending on whether or not the writing size is large enough for 8 times in units of 512 B; that is, whether or not the writing size is larger than 4 KB. Moreover, referring to the entry table shown in Fig. 47(b), a block corresponding to an invalid block (11 in binary) is specified as an erasing target block. By the process thus far described, in the case

where the writing size for the nonvolatile memory chip A is greater than or equal to 4 KB, the time for erasing of the nonvolatile memory chip B is cut back with consequent accomplishment of a rationalization of the entire processing performance. Further, by deriving a quotient of a capacity corresponding to writing size "L" (L sector × 512 B) and 4 KB (refer to Fig. 8), as much writing operation as possible can be conducted without causing deterioration in processing performance. Although, in Fig. 50, there is shown the case of writing to the nonvolatile memory chip A (erasing of the nonvolatile memory chip B), according to the flow chart shown in Fig. 49, the process is applicable also to the case of writing to the nonvolatile memory chip B (erasing of the nonvolatile memory chip A) or the case of writing across the first and latter half areas (across the nonvolatile memory chips A and B).

[0109]

It is noted that the nonvolatile memory chips A and B may be connected to the memory controller 4602 by a single common bus. In this case, however, to avoid bus contention between a write command and an erase command as shown in Fig. 50, the nonvolatile memory access section 123 effects control to stagger write command issuance timing and erase command issuance timing. Moreover, in the logical-to-

physical conversion table shown in Fig. 47(a), conversion may be made on a block-by-block basis. Also, when a plurality of erase blocks are grouped, conversion may be made on a group-by-group basis (in these cases, the process shown in Fig. 49 needs to be adapted for such a block-by-block or group-by-group operation. Furthermore, the logical-to-physical conversion table and the entry table may employ a reading-writing memory other than RAM as long as it allows relatively fast access. In addition, although the third embodiment deals with the case where the nonvolatile memory 4601 takes on a two-chip structure; that is, has the nonvolatile memory chips A and B for parallel access, the nonvolatile memory 4601 may be formed of a single nonvolatile memory chip. In this case, the nonvolatile memory access section 123 is designed to exercise serial switching control such that pre-erasing is conducted (erasing is conducted prior to writing) for writing in substantial writing size of, e.g. 16 KB, whereas pre-erasing is not conducted for writing in relatively small capacity. In this case, in contrast to the case where no switching control is exercised (i.e. pre-erasing is imperative regardless of writing size), processing performance can be normally improved.

[0110]

(Fourth embodiment)

Figure 51 is a diagram showing how the fourth embodiment of the present invention is to be carried into effect. In Fig. 51, numerical symbol 5101 represents a nonvolatile memory wherein two pieces of nonvolatile memory elements (nonvolatile memory chip A and nonvolatile memory chip B) exist. 5102 represents a logical-to-physical conversion control section, 5103 represents a nonvolatile memory access section, and 5104 represents a memory controller. Other blocks are similar to those shown in Fig. 1. Note that the nonvolatile memory chip A and the nonvolatile memory chip B are connected to the memory controller 5104 by independent bidirectional buses, respectively.

[0111]

Figure 52 is an explanatory view showing the internal configurations of the nonvolatile memory chips A and B. The nonvolatile memory chips A and B within the nonvolatile memory 5101 are each divided into four banks, and the banks 0 to 3 are capable of writing concurrently on a page-by-page basis. Each erase block (4 KB = 4224 B) consists of two pages (segment represented by hatching is the page). A group of 8 erase blocks in total, of which each is provided per bank in the nonvolatile memory chips A and B, is defined as a logical section, and the nonvolatile memory 5101 in its entirety consists of 256 sections.

[0112]

Figure 53 is an explanatory view showing a logical address format. A bit corresponding to a logical section No. is a target of logical-to-physical conversion.

[0113]

Figure 54 is an explanatory view showing the logical-to-physical conversion control section 5102. The logical-to-physical conversion control section 5102 is a table for managing process of conversion from a logical address specified by the access device 100 to a physical address and the state of each physical block. Fig. 54(a) shows a logical-to-physical conversion table for converting a logical section No. to a physical section No. Fig. 54(b) shows an entry table indicating whether each physical block is valid or invalid, or a defective block. Both of the logical-to-physical conversion table and the entry table are stored in a volatile memory such as RAM. Note that the logical-to-physical conversion table shown in Fig. 54(a) and the entry table shown in Fig. 54(b) are produced on the RAM within the logical-to-physical conversion control section 5102 by reading information stored in the management area of each erase block of the nonvolatile memory chips A and B by the CPU 113 at the time of initialization immediately after power-up.

[0114]

Figure 55 is an explanatory view showing the configuration of the erase block. The erase block consists of two pages, and each page has a capacity of 2112 bytes that is the sum of 2048 bytes (data area) and 64 bytes (management area). Here, in the management area in the page 0 of the erase block present in the bank 0 of the nonvolatile memory chip A, as so-called link information, physical address information on the erase blocks of the banks 1 to 3 of the nonvolatile memory chip A and the banks 0 to 3 of the nonvolatile memory chip B is stored for formation of a physical section corresponding to the logical section. Moreover, like the third embodiment, address management information including a logical address corresponding to the user data written on the data area and a flag indicating whether the data is valid or invalid, or a defective block is also written. Note that the information for section management such as the link information may be stored in an erase block other than the erase block present in the bank 0 of the nonvolatile memory chip A.

[0115]

Figure 56 is a time chart for the case where the speed mode set in the host information storage part 125 by the access device 100 is a high-speed mode (the magnitude of peak current is relatively large).

[0116]

Figure 57 is a time chart for the case where the speed mode set in the host information storage part 125 by the access device 100 is a low-speed mode (the magnitude of peak current is relatively small).

[0117]

Referring mainly to Figs. 56 and 57, the semiconductor memory card and the access device thereby constructed will be described in respect of their workings. Firstly, at the time of initialization after power-up in the access device 100 or upon switching or the like operation on the access device 100, the speed mode transferred to be stored in the host information storage part 125. Then, the nonvolatile memory access section 5103 changes the form of access with reference to the speed mode stored in the host information storage part 125. In the case of the high-speed mode (Fig. 56), the writing data A, B, C, D, …… (assumed to be continuous logical addresses) transferred from the access device 100 are transferred via the host interface 112 and the logical-to-physical conversion control section 5102 to the nonvolatile memory access section 5103, and are successively written to the nonvolatile memory chips A and B via the bus No. 0 and the bus No. 1 in units of 8 KB. On the other hand, in the case where the speed mode set in the host information storage

part 125 is the low-speed mode, as shown in Fig. 57, the writing data A, B, C, D, ... are subjected to writing control to avoid overlap of the program busy time (time period that consumes a larger amount of power than does other time such as the data transfer time) at one bus and the program busy time at the other bus. Specifically, the nonvolatile memory access section 5103 feeds a card busy signal back to the access device 100 to effect a wait for data transfer until it is informed of cancellation of program busy signals for the nonvolatile memory chips A and B targeted for writing. By exercising such a bidirectional control, the program busy time periods (in which a large amount of power is consumed) can be distributed with consequent accomplishment of peak current regulation. Therefore, in the case of using the access device 100 having a power supply circuit with a low withstand current value, since the low-speed mode should be selected, the access device 100 establishes the low-speed mode in the host information storage part 125. On the other hand, in the case of using the access device 100 having a power supply circuit with a high withstand current value, when high-rate access is requested, the high-speed mode is set in the host information storage part 125. In response to setting condition, the nonvolatile memory access section 123 makes a selection between the access form shown in Fig.

56 and that shown in Fig. 57 and effects writing control according to the selected access form.

[0118]

It is noted that the logical-to-physical conversion table and the entry table may employ a reading-writing memory other than RAM as long as it allows relatively fast access.

[0119]

(Fifth embodiment)

Figure 58 is a diagram showing how the fifth embodiment of the present invention is to be carried into effect. In Fig. 58, numerical symbol 5801 represents a nonvolatile memory, 5802 represents a logical-to-physical conversion control section, 5803 represents a nonvolatile memory access section, and 5804 represents a memory controller. Other blocks are similar to those shown in Fig. 1.

[0120]

Figure 59 is an explanatory view showing the internal configuration of the nonvolatile memory 5801. The nonvolatile memory 5801 is divided into four banks, and the banks 0 to 3 are capable of writing concurrently on a page-by-page basis. Each erase block (16896 B ≒ 16 KB) consists of 32 pages. The erase block is similar in configuration to that of Third embodiment as shown in Fig.

48.

[0121]

Figure 60 is an explanatory view showing the logical-to-physical conversion control section 5802. The logical-to-physical conversion control section 5802 is subjected to switching control on the basis of a logical-to-physical conversion through flag transferred to and recorded on the host information storage part 125 by the access device 100. In Fig. 60(a), 6001 represents a logical-to-physical conversion table for converting a logical block address to a physical block address, and 6002 represents a selector for transferring a logical address to the nonvolatile memory access section 5803 as a physical address without processing when the logical-to-physical conversion through flag is in an active state (e.g. value 1). Fig. 60(b) shows an entry table indicating whether each physical block is valid or invalid, or a defective block. Both of the logical-to-physical conversion table and the entry table are stored in a volatile memory such as RAM. Note that the logical-to-physical conversion table 6001 shown in Fig. 60(a) and the entry table shown in Fig. 60(b) are produced on the RAM within the logical-to-physical conversion control section 5802 by reading information stored in the management area of each erase block of the nonvolatile memory 5801 by the CPU 113 at the time of initialization

immediately after power-up.

[0122]

Figure 61 is an explanatory view showing the internal configuration of the logical-to-physical conversion table 6001.

[0123]

Referring mainly to Figs. 59 and 60, the semiconductor memory card and the access device thereby constructed will be described in respect of their workings. In Fig. 60, when the logical-to-physical conversion through flag is in an inactive state, that is, when logical-to-physical conversion takes place, then the individual physical blocks of the nonvolatile memory 5801 shown in Fig. 59 are subjected to conversion process on a physical block-by-physical block basis without any particular regularity unless section management such as adopted in the fourth embodiment (a plurality of physical blocks are grouped and management is conducted by the group) is performed. Therefore, for example, it could be that all of the blocks of the bank 1 (indicated by a broken line in Fig. 59) will become valid. In this case, the number of pages for concurrent writing is limited. Specifically, concurrent writing can be performed only in the pages of a bank other than the bank 1, namely the banks 0, 2, and 3, wherefore the writing rate becomes lower as compared with the case

where all of the banks 0, 1, 2, and 3 are capable of concurrent writing. As a way to avoid this problem, the omission of logical-to-physical conversion can be considered. By doing so, the workings can be controlled at the side of the access device 100 in such a manner that the banks 0 to 3 are constantly in a writable state; that is, the blocks of a given bank will not become all valid. Here, in a system that employs a flash memory for the nonvolatile memory 5801 and may pose the possibility of concentration of writings on a part of the entire area of the flash memory, wear leveling (avoidance of rewriting concentration), or logical-to-physical conversion is required. However, in a system in which all the areas are subjected to writing at a stroke in many cases such as a moving image recording-reproducing apparatus designed for long-duration recording, in contrast to a system which allows random rewriting with a small capacity, the need for installation of a wear leveling mechanism (logical-to-physical conversion) is low. Furthermore, if a nonvolatile memory which operates without limitation on the number of rewritings and is nevertheless suitable for practical use from the standpoints of capacity and cost is developed in the future, the installation of the wear leveling mechanism (logical-to-physical conversion) will no longer be necessary. With consideration given to this fact, when it

is determined that wear leveling such as mentioned above is not very necessary or not necessary (instead, when it is determined that physical block management at the access device side is more suitable for high-rate access) on the basis of an instruction from the access device 100, by establishing the logical-to-physical conversion through flag in the host information storage part 125, the workings can be controlled at the side of the access device 100 so as to avoid a decrease in writing rate. As an advantage at the side of the memory controller 5804 (realized by using LSI, for example), switching control can be exercised as to whether or not the logical-to-physical conversion control section 5802 performs logical-to-physical conversion. Thus, the semiconductor memory card and the access device can be versatilely used in keeping with the needs for high-speed performance and long-life nature of a nonvolatile memory (wear leveling) regardless of application purposes and types of nonvolatile memories to be mounted.

[0124]

It is noted that by providing feedback on concurrent writing conditions (the number of banks and page size or the number of nonvolatile memories capable of parallel processing) stored in the card information storage part 124 to the access device 100, the management of the nonvolatile memory 5801 by the access device 100 can be facilitated.

Moreover, the logical-to-physical conversion table 6001 and the entry table may employ a reading-writing memory other than RAM as long as it allows relatively fast access. Further, the nonvolatile memory 5801 may have a plurality of built-in nonvolatile memory chips.

[0125]

(Sixth embodiment)

Figure 62 is a diagram showing how the sixth embodiment of the present invention is to be carried into effect. In Fig. 62, numerical symbol 6201 represents a nonvolatile memory, 6202 represents a logical-to-physical conversion control section, 6203 represents a free physical area generating section, 6204 represents a nonvolatile memory access section, and 6205 represents a memory controller. Other blocks are similar to those shown in Fig. 1. Note that the free physical area generating section 6203 acts to increase the number of free blocks (erase blocks) by organizing the state of recording within the nonvolatile memory 6201 for writing at anytime without the necessity of pre-erasing. Moreover, the erase block within the nonvolatile memory 6201 is similar to that of the third embodiment shown in Fig. 48.

[0126]

Figure 63 is an explanatory view showing the logical-to-physical conversion control section 6202. The logical-

to-physical conversion control section 6202 is a table for managing process of conversion from a logical address specified by the access device 100 to a physical address and the state of each physical block. Fig. 63(a) shows a logical-to-physical conversion table for converting a logical sector address to a physical sector address. Fig. 63(b) shows an entry table indicating whether each physical block is valid or invalid, or a defective block, or a free block (erased block), or a defragmentation target block. Both of the logical-to-physical conversion table and the entry table are stored in a volatile memory such as RAM. Note that the logical-to-physical conversion table shown in Fig. 63(a) and the entry table shown in Fig. 63(b) are produced on the RAM within the logical-to-physical conversion control section 6202 by reading information stored in the management area of each erase block of the nonvolatile memory 6201 by the CPU 113 at the time of initialization immediately after power-up.

[0127]

Figure 64 is an explanatory view showing defragmentation process.

[0128]

Referring mainly to Fig. 64, the semiconductor memory card and the access device thereby constructed will be described in respect of their workings. As the access

device 100 transfers instructions including writing commands one after another to the semiconductor memory card, the number of free blocks in the nonvolatile memory 6201 is gradually reduced. In the sixth embodiment, in contrast to the fourth embodiment (refer to Fig. 53), the sectors (pages) in the erase block are not written upon in logical order, and logical sectors transferred by the access device 100 are written in a descending sequence to the erase block regardless of their logical sector addresses. Specifically, as shown in Fig. 64, when the access device 100 permits writing in the logical sectors 4, 0, 0, 1, 3 ……, then writing is performed in a descending sequence at the positions of the sector numbers 0, 1, 2, 3 …… of the erase block 1. Upon a certain number of sectors being written to the erase block, the free block area generating section 6203 registers the erase block as a defragmentation target block to the entry table shown in Fig. 63(b). Then, logical sectors newly transferred by the access device 100 are written to another free block (erased block) searched with reference to the entry table. As such an operation goes on, the number of free blocks in the entry table is gradually reduced but at the same time the number of defragmentation target blocks is gradually increased. For example, the free block area generating section 6203 has a counter for keeping count of the number of free blocks in

the entry table and, when a count value falls below a predetermined level, returns a defragmentation request signal or the count value to the access device 100. The access device 100 may transfer a defragmentation instruction signal to the semiconductor memory card 111 immediately after the reception of the defragmentation request signal, or may issue a defragmentation instruction signal after ascertaining the timing of defragmentation instruction signal transfer in consideration of the capacity of data to be transferred afterwards on the basis of the aforementioned count value. A defragmentation instruction signal transferred from the access device 100 is temporarily stored in the host information storage part 125. With reference to this defragmentation instruction signal, the free physical area generating section 6203 issues a defragmentation process instruction to the nonvolatile memory access section 6204. Specifically, as shown in Fig. 64, looking at the sector numbers (sectors marked with a flag "new" only) of each of the erase blocks 1 and 5 (both blocks have been registered as defragmentation target blocks), a reading-writing instruction is issued to the nonvolatile memory access section 6204 so that merging can be performed on the free block 9 in the order of the logical sectors. In response to the instruction, as shown in Fig. 64, the nonvolatile

memory access section 6204 effects copyback of logical sectors with a flag "new" in the erase blocks 1 and 5 toward the erase block 9 which is a free block. Note that, like the fourth embodiment (refer to Fig. 53), in the case where the memory controller 5104 defines a logical format in which the sectors (pages) of an erase block are arranged in logical order in the erase block without fail, the free physical area generating section 121 does not perform defragmentation process such as mentioned above but only issues an instruction for erasing invalid blocks of the entry table shown in Fig. 22(b) to the nonvolatile memory access section 123. Note that the logical-to-physical conversion table and the entry table may employ a reading-writing memory other than RAM as long as it allows relatively fast access. Moreover, the nonvolatile memory 6201 may have a plurality of built-in nonvolatile memory chips.

[0129]

(Seventh embodiment)

Figure 65 is a diagram showing how the seventh embodiment of the present invention is to be carried into effect. In Fig. 65, numerical symbol 6501 represents a nonvolatile memory, 6502 represents a logical-to-physical conversion control section, 6503 represents a nonvolatile memory access section, and 6504 represents a memory

controller. Other blocks are similar to those shown in Fig. 1. Note that the logical-to-physical conversion control section 6502 is constructed by storing both the logical-to-physical conversion table shown in Fig. 61 and the entry table shown in Fig. 60(b) of the fifth embodiment in a volatile memory such as RAM. Moreover, the logical-to-physical conversion table and the entry table are copied on the RAM within the logical-to-physical conversion control section 6502 by reading AT on an AT area of the nonvolatile memory 6501 (as will hereafter be described) by the CPU 113 at the time of initialization immediately after power-up.

[0130]

Figure 66 is an explanatory view showing the internal configuration of the nonvolatile memory 6501. The specifications of erase blocks and pages in the nonvolatile memory 6501 are similar to those in the semiconductor memory chip A of the fourth embodiment (Fig. 52).

[0131]

Figure 67 is an explanatory view showing the access form of a conventional nonvolatile memory access section.

[0132]

Figure 68 is an explanatory view showing the access form of the nonvolatile memory access section 6503.

[0133]

Referring mainly to Figs. 66 to 68, the semiconductor

memory card and the access device thereby constructed will be described in respect of their workings. Firstly, the nonvolatile memory 6501 shown in Fig. 66 differs in configuration from the nonvolatile memories of the third to sixth embodiments. In this construction, the address management information 126 is stored in a format of the type of the logical-to-physical conversion table and the entry table on an AT area within the nonvolatile memory 6501 and is thus copied on the RAM within the logical-to-physical conversion control section 6502 when the CPU 113 effects reading at the time of initialization. Note that "AT" is an abbreviation for "allocation table" which is required for the memory controller 6504 to manage the nonvolatile memory 6501. The purpose of collective recording of AT in an area other than the data area is as follows. In the case where quite a few erase blocks are present in the nonvolatile memory 6501, if, like the third to sixth embodiments, the logical-to-physical conversion table and the entry table are produced on the RAM at the time of initialization on the basis of the management information on the management area of each erase block, relatively much time will be required. When it is necessary to save the time (i.e. in the case of using a nonvolatile memory having quite a few erase blocks), such an AT management method is adopted. In this case, in the

access form of a conventional nonvolatile memory access section, as shown in Fig. 67, a process step of updating AT on the RAM and writing it back to the nonvolatile memory for each writing command from the access device 100 (AT write as shown in Fig. 67) is required. Incidentally, AT read may be conducted only at the time of initialization unless the data area of the nonvolatile memory 6501 is managed in a divided state (i.e. when AT manages all the data areas). Temporal overhead entailed by the AT write gives rise to a problem peculiar to the seventh embodiment 7 (deterioration in processing performance), and it becomes problematic especially in the case where the capacity of data write is small, in other words, the proportion of AT write time to the entire processing time (data write time + AT write time) is relatively large. In order to solve this problem, in the seventh embodiment, an AT update instruction signal as shown in Fig. 68 is used. The AT update instruction signal is a signal which is issued by the access device 100. For example, in a system in which the access device 100 effects consecutive writing of user data having a size of the order of several hundreds KB and FAT update at the side of the access device 100 is made in the order of several hundreds KB, AT update may also be made in accordance with its span. This is because, for example, when the power is shut off before the completion

of FAT update (writing to the nonvolatile memory 6501), the FAT remains unupdated and thus there is no need for AT update. Instead, it can be said that it is more reasonable to provide a match between FAT update and AT update. In the access device 100, the FAT update span varies according to its application purposes. Therefore, to achieve processing performance optimization according to application purposes (specifications of the access device 100), it is advisable to control AT update timing (transfer AT update instruction signal) at the side of the access device 100.

[Industrial Applicability]

[0134]

A semiconductor memory card, access device, and access method pursuant to the present invention can realize high-rate access to a semiconductor memory card by optimizing process at the side of the access device or semiconductor memory card, or process at both sides. Such semiconductor memory card, and access device and method can be used in digital AV equipment, cellular phone terminals, PCs, etc., that use the semiconductor memory card as a recording medium. Furthermore, they work suitably especially when used in a recording medium and equipment that record high-quality AV data with high transfer rate.

[Brief Description of Drawings]

[0135]

[Fig. 1] Fig. 1 is an explanatory view showing how a semiconductor memory card and an access device in accordance with the first embodiment of the present invention are to be carried into effect.

[Fig. 2] Fig. 2 is an explanatory view showing an example of relationship between an erase block and a sector in accordance with the first embodiment of the present invention.

[Fig. 3] Fig. 3 is a flow chart showing process of writing data having a length of multiples of the erase block to the semiconductor memory card in accordance with the first embodiment of the present invention.

[Fig. 4] Fig. 4 is a flow chart showing process of writing data by 1 sector to the semiconductor memory card in accordance with the first embodiment of the present invention.

[Fig. 5] Fig. 5 is an explanatory view showing an example of the configuration of the semiconductor memory card using two Flash memories in accordance with the first embodiment of the present invention.

[Fig. 6] Fig. 6 is an explanatory view showing an example of access timing of the semiconductor memory card using the two Flash memories in accordance with the first embodiment of the present invention.

[Fig. 7] Fig. 7 is an explanatory view showing information stored in a card information storage part in accordance with the first embodiment of the present invention.

[Fig. 8] Fig. 8 is a flow chart showing internal process of the access device in the first method in accordance with the first embodiment of the present invention.

[Fig. 9] Fig. 9 is a flow chart showing internal process of the semiconductor memory card in the first method in accordance with the first embodiment of the present invention.

[Fig. 10] Fig. 10 is an explanatory view showing an example of access conditions and access rate values in the first method in accordance with the first embodiment of the present invention.

[Fig. 11] Fig. 11 is a flow chart showing internal process of the access device in the second method in accordance with the first embodiment of the present invention.

[Fig. 12] Fig. 12 is a flow chart showing internal process of the semiconductor memory card in the second method in accordance with the first embodiment of the present invention.

[Fig. 13] Fig. 13 is an explanatory view showing an

example of access conditions and access rate values in the second method in accordance with the first embodiment of the present invention.

[Fig. 14] Fig. 14 is a flow chart showing internal process of the access device in the third method in accordance with the first embodiment of the present invention.

[Fig. 15] Fig. 15 is a flow chart showing internal process of the semiconductor memory card in the third method in accordance with the first embodiment of the present invention.

[Fig. 16] Fig. 16 is a flow chart showing internal process of the access device in the fourth method in accordance with the first embodiment of the present invention.

[Fig. 17] Fig. 17 is a flow chart showing internal process of the semiconductor memory card in the fourth method in accordance with the first embodiment of the present invention.

[Fig. 18] Fig. 18 is an explanatory view showing an example of the level determination criteria of rate performance in the fifth method in accordance with the first embodiment of the present invention.

[Fig. 19] Fig. 19 is a flow chart showing internal process of the semiconductor memory card in the sixth

method in accordance with the first embodiment of the present invention.

[Fig. 20] Fig. 20 is a flow chart showing internal process of the access device in the seventh method in accordance with the first embodiment of the present invention.

[Fig. 21] Fig. 21 is a flow chart showing internal process of the semiconductor memory card in the seventh method in accordance with the first embodiment of the present invention.

[Fig. 22] Fig. 22 is an explanatory view showing an example of the access performance basic information list in the seventh method in accordance with the first embodiment of the present invention.

[Fig. 23] Fig. 23 is an explanatory view showing an example of access timing between the access device and the semiconductor memory card in reading process and writing process in the seventh method in accordance with the first embodiment of the present invention.

[Fig. 24] Fig. 24 is an explanatory view showing an example of the access timing between the access device and the semiconductor memory card in erasing process in the seventh method in accordance with the first embodiment of the present invention.

[Fig. 25] Fig. 25 a flow chart showing internal

process of the access device in the eighth method in accordance with the first embodiment of the present invention.

[Fig. 26] Fig. 26 is a flow chart showing internal process of the semiconductor memory card in the eighth method in accordance with the first embodiment of the present invention.

[Fig. 27] Fig. 27 is an explanatory view showing an example of an access performance table using data size which can be processed per unit time in the eighth method in accordance with the first embodiment of the present invention.

[Fig. 28] Fig. 28 is an explanatory view showing an example of the access performance table using required time for data process of a unit size in the eighth method in accordance with the first embodiment of the present invention.

[Fig. 29] Fig. 29 is an explanatory view showing an example of the access performance table in the eighth method in accordance with the first embodiment of the present invention.

[Fig. 30] Fig. 30 is an explanatory view showing the configuration of a FAT file system in accordance with the second embodiment of the present invention.

[Fig. 31] Fig. 31 is an explanatory view showing an

example of data storage of the FAT file system in accordance with the second embodiment of the present invention.

[Fig. 32] Fig. 32 is a flow chart showing data writing process of the FAT file system in accordance with the second embodiment of the present invention.

[Fig. 33] Fig. 33 is an explanatory view showing a state before data writing of the FAT file system in accordance with the second embodiment of the present invention.

[Fig. 34] Fig. 34 is an explanatory view showing a state after data writing of the FAT file system in accordance with the second embodiment of the present invention.

[Fig. 35] Fig. 35 is a flow chart showing FS access unit acquisition process in accordance with the second embodiment of the present invention.

[Fig. 36] Fig. 36 is an explanatory view showing a configuration example of formatted file system using an FS access unit in the first method in accordance with the second embodiment of the present invention.

[Fig. 37] Fig. 37 is a flow chart showing the writing process of file data using the FS access unit in the second method in accordance with the second embodiment of the present invention.

[Fig. 38] Fig. 38 is an explanatory view showing an example of data arrangement in the second method in accordance with the second embodiment of the present invention.

[Fig. 39] Fig. 39 is a flow chart showing the directory area allocation process using the FS access unit in the third method in accordance with the second embodiment of the present invention.

[Fig. 40] Fig. 40 is an explanatory view showing an example of data arrangement in the third method in accordance with the second embodiment of the present invention.

[Fig. 41] Fig. 41 is an explanatory view showing an example of data arrangement before defragmentation process using the FS access unit in the fourth method in accordance with the second embodiment of the present invention.

[Fig. 42] Fig. 42 is an explanatory view showing an example of data arrangement after defragmentation process using the FS access unit in the fourth method in accordance with the second embodiment of the present invention.

[Fig. 43] Fig. 43 is a flow chart showing the remaining free area length acquisition process using the FS access unit in the fifth method in accordance with the second embodiment of the present invention.

[Fig. 44] Fig. 44 is an explanatory view showing an

example of data arrangement in the fifth method in accordance with the second embodiment of the present invention.

[Fig. 45] Fig. 45 is an explanatory view showing how the semiconductor memory card using a semiconductor memory card control LSI and access device in accordance with the second embodiment of the present invention are to be carried into effect.

[Fig. 46] Fig. 46 is an explanatory view showing how the semiconductor memory card and access device in accordance with the third embodiment of the present invention are to be carried into effect.

[Fig. 47] Fig. 47 is an explanatory view showing a logical-to-physical conversion control section 118 in accordance with the third embodiment of the present invention.

[Fig. 48] Fig. 48 is an explanatory view showing the configuration of an erase block in accordance with the third embodiment of the present invention.

[Fig. 49] Fig. 49 is a flow chart showing process in the free physical area generating section 121 in accordance with the third embodiment of the present invention.

[Fig. 50] Fig. 50 is a time chart showing the form of access from the nonvolatile memory access section 123 to the nonvolatile memory 501 in accordance with the third

embodiment of the present invention.

[Fig. 51] Fig. 51 is an explanatory view showing how the semiconductor memory card and access device in accordance with the fourth embodiment of the present invention are to be carried into effect.

[Fig. 52] Fig. 52 is an explanatory view showing the internal configuration of nonvolatile memory chips A and B in accordance with the fourth embodiment of the present invention.

[Fig. 53] Fig. 53 is an explanatory view showing logical address format in accordance with the fourth embodiment of the present invention.

[Fig. 54] Fig. 54 is an explanatory view showing a logical-to-physical conversion control section 1002 in accordance with the fourth embodiment of the present invention.

[Fig. 55] Fig. 55 is an explanatory view showing the configuration of an erase block in accordance with the fourth embodiment of the present invention.

[Fig. 56] Fig. 56 is a time chart for a high-speed mode in accordance with the fourth embodiment of the present invention.

[Fig. 57] Fig. 57 is a time chart for a low-speed mode in accordance with the fourth embodiment of the present invention.

[Fig. 58] Fig. 58 is an explanatory view showing how the semiconductor memory card and access device in accordance with the fifth embodiment of the present invention are to be carried into effect.

[Fig. 59] Fig. 59 is an explanatory view showing the internal configuration of a nonvolatile memory 1701 in accordance with the fifth embodiment of the present invention.

[Fig. 60] Fig. 60 is an explanatory view showing a logical-to-physical conversion control section 1702 in accordance with the fifth embodiment of the present invention.

[Fig. 61] Fig. 61 is an explanatory view showing the internal configuration of a logical-to-physical conversion table 1901 in accordance with the fifth embodiment of the present invention.

[Fig. 62] Fig. 62 is an explanatory view showing how the semiconductor memory card and access device in accordance with the sixth embodiment of the present invention are to be carried into effect.

[Fig. 63] Fig. 63 is an explanatory view showing a logical-to-physical conversion control section 2102 in accordance with the sixth embodiment of the present invention.

[Fig. 64] Fig. 64 is an explanatory view showing

defragmentation process in accordance with the sixth embodiment of the present invention.

[Fig. 65] Fig. 65 is an explanatory view showing how the semiconductor memory card and access device in accordance with the seventh embodiment of the present invention are to be carried into effect.

[Fig. 66] Fig. 66 is an explanatory view showing the internal configuration of a nonvolatile memory 2401 in accordance with the seventh embodiment of the present invention.

[Fig. 67] Fig. 67 is an explanatory view showing the access form of a conventional nonvolatile memory access section in accordance with the seventh embodiment of the present invention.

[Fig. 68] Fig. 68 is an explanatory view showing the access form of a nonvolatile memory access section 2403 in accordance with the seventh embodiment of the present invention.

[Explanation of reference designations]

[0136]

100 access device

101, 113 CPU

102, 114 RAM

103 slot

104, 115 ROM

105 application program

106 file system control part

107 access condition determination part

108 card information acquisition part

109 access control part

110 card use condition storage part

111 semiconductor memory card

112 host interface

116 memory controller

117 nonvolatile memory

118 first memory

119 second memory

120 logical-to-physical conversion control section

121 free physical area generating section

122 address management information update control section

123 nonvolatile memory access section

124 card information storage part

125 host information storage part

126 address management information

127 user data

Fig.1

100 Access device

101, 113 CPU

102, 114 RAM

103 Slot

104, 115 ROM

105 Application program

106 File system control part

107 Access condition determination part

108 Card information acquisition part

109 Access control part

110 card use condition storage part

111 Semiconductor memory card

112 Host interface

116 Memory controller

117 Nonvolatile memory

118 First memory

119 Second memory

120 Logical-to-physical conversion control section

121 Free physical area generating section

122 Address management information update control section

123 Nonvolatile memory access section

124 Card information storage part

125 Host information storage part

126 Address management information

127 User data

Fig.2

physical sector numbers

flash memory

erase block 0

erase block 1

erase block (N-1)

Fig.3

S301 Receive command

S302 Incorrect command?

S303 Error finish

S304 Writing command?

S305 Perform other process

S306 Determine physical address

S307 Erase data for 1 erase block

S308 Receive data for 1 sector

S309 Write data for 1 sector

S310 Writing for 1 erase block finished?

S311 Writing all data finished?

Fig.4

S401 Receive command

S402 Incorrect command?

S403 Error finish

S404 Writing command

S405 Perform other process

S406 Determine physical address

S407 Erase data for 1 erase block

S408 Receive data for 1 sector

S409 Write data for 1 sector

S410 Writing for (1 erase block - 1 sector)

Fig.5

flash memory 0

flash memory 1

erase block 0_0

erase block 0_1

erase block 0_(N-1)

erase block 1_0

erase block 1_1

erase block 1_(N-1)

PSN: physical sector number

Fig.6

(a) Timing of writing data of one erase block

Input to card

Write command

Data 1

Output from card

Response

Busy (Writing data 1)

(b) Timing of writing data of two erase blocks

Input to card

Write command

Data 1

Data 2

Output from card

Response

Busy

Busy (Writing data 1, 2)

Fig.7

Types

Items

Information on internal physical characteristics

Memory type (Flash, MRAM etc)

Number of Flash memory used in the semiconductor memory card

Management method of the semiconductor memory such as presence or absence of parallel writing to the memory

Erase block size

Management block size

Temperature conditions

Power consumption

Current value

Voltage value

Card type information (such as version supported command set)

Information on access conditions

Process type (read/write/erase, etc)

Process unit size

Process unit boundary

Process unit time

Access method (sequential/random)

Minimum sequential area size at sequential access

Input clock frequency

Bit width (1 bit/4 bit etc)

Information on the access performance

Rate performance level (high/middle/low)

Data size to be processed within unit time

Required time for processing per unit size

Transfer rate

Process time inside card (Read access time, Write/Erase busy time, etc)

Information on abnormal process

Error occurrence probability

Worst value of error notification time

Other information

Rate performance level determination reference

Rate performance level

Power consumption level

Fig.8

S801 Issue card type acquisition command

S802 Card type acquisition successful?

S803 Error finish

S804 Card corresponding to optimum access information acquisition command?

S805 Cancel information acquisition

S806 Issue optimum access information acquisition command

S807 Information acquisition successful?

S808 Error finish

Fig.9

S901 Receive command

S902 Incorrect command?

S903 Error finish

S904 Card type acquisition command?

S905 Perform other process

S906 Read from the card information from card information storage part

S907 Transmit the read information to the access device

S908 Receive command

S909 Incorrect command?

S910 Error finish

S911 Optimum access information acquisition command?

S912 Perform other process

S913 Read access conditions for optimally accessing and access performance values from card information storage part

S914 Transmit the read information to the access device

Fig.10

(a) Access condition

Items

Process unit size

Process unit boundary

Access method

Input clock frequency

Bit width

Condition values

Multiple length of 128KB

Multiple length of 128KB

Sequentially accessing to sequential area having 256KB over

4 bits

(b) Access performance values

Transfer rate of reading (standard) = 11MB/s

Transfer rate of writing (standard) = 10MB/s

Transfer rate of erasing (standard) = 10.3MB/s

Transfer rate of reading (worst) = 6MB/s

Transfer rate of writing (worst) = 5MB/s

Transfer rate of erasing (worst) = 5.1MB/s

Fig.11

S1101 Issue card type acquisition command

S1102 Card type acquisition successful?

S1103 Error finish

S1104 Is this a card corresponding to optimum access information acquisition command?

S1105 Cancel access rate value acquisition

S1106 Issue access rate value command

S1107 Access rate value acquisition successful?

S1108 Error finish

Fig.12

S1201 Receive command

S1202 Incorrect command?

S1203 Error finish

S1204 Card corresponding to access rate value acquisition command?

S1205 Perform other process

S1206 Read access condition and access performance value from information storage part

S1207 Judge if access condition which access device designates exist referring to read access conditions and corresponding access performance value

S1208 Does access performance value exist?

S1209 Error finish

S1210 Transmit access rate value to access device

Fig.13

(a) Access condition

Items

Process unit size

Process unit boundary

Access method

Input clock frequency

Bit width

Condition values

Sequentially accessing to sequential area having 256KB

4 bits

(b) Access performance values

Transfer rate of reading (standard) = 11MB/s

Transfer rate of writing (standard) = 10MB/s

Transfer rate of erasing (standard) = 10.3MB/s

Transfer rate of reading (worst) = 6MB/s

Transfer rate of writing (worst) = 5MB/s

Transfer rate of erasing (worst) = 5.1MB/s

Fig.14

S1401 Issue card type acquisition command

S1402 Card type acquisition successful?

S1403 Error finish

S1404 Is this a card corresponding to access condition acquisition command?

S1405 Cancel access condition acquisition

S1406 Issue access condition command

S1407 Access condition acquisition successful?

S1408 Error finish

Fig.15

S1501 Receive command

S1502 Incorrect command?

S1503 Error finish

S1504 Access condition acquisition command?

S1505 Perform other process

S1506 Read access conditions and access performance values from card information storage part

S1507 Judges if access condition corresponding access performance value which the access device designates exist or not based on read access condition

S1508 Existing access condition?

S1509 Error finish

S1510 Transmit access condition to access device

Fig.16

S1601 Issue card type acquisition command

S1602 Card type acquisition successful?

S1603 Error finish

S1604 Is this a card corresponding to optimum access propriety determination command?

S1605 Cancel optimum access propriety determination

S1606 Issue optimum access propriety determination command

S1607 Determination result acquisition successful?

S1608 Error finish

Fig.17

S1701 Receive command

S1702 Incorrect command?

S1703 Error finish

S1704 Optimum access propriety determination command?

S1705 Perform other process

S1706 Read access condition and access performance value from information storage part

S1707 It is determine the access performance value is met referring to the thereby read access conditions and corresponding access performance values

S1708 Meet performance value?

S1709 The fact that the access performance value is met is informed to the access device

S1710 The fact that the access performance value is not met

Fig.18

(a) Rate performance level determination criteria

Rate performance level
High
Medium
Low
Reading
Standard transfer rate >= 8.0MB/s

4.0Mb/s =< Standard transfer rate <= 8.0MB/s

Standard transfer rate < 4.0MB/s

Writing

Standard transfer rate >= 8.0MB/s

4.0Mb/s =< Standard transfer rate <= 8.0MB/s

Standard transfer rate < 4.0MB/s

Erasing

Standard transfer rate >= 8.0MB/s

4.0Mb/s =< Standard transfer rate <= 8.0MB/s

Standard transfer rate < 4.0MB/s

(b) Access performance value

Access performance values

Transfer rate

Transfer rate of reading (standard) = 11MB/s

Transfer rate of writing (standard) = 10MB/s

Transfer rate of erasing (standard) = 10.3MB/s

Transfer rate of reading (worst) = 6MB/s

Transfer rate of writing (worst) = 5MB/s

Transfer rate of erasing (worst) = 5.1MB/s

Rate performance level

High

High

High

High

High

High

Fig.19

S1901 Receive command

S1902 Incorrect command?

S1903 Error finish

S1904 Optimum access information acquisition command?

S1905 Perform other process

S1906 Designated power consumption level valid?

S1907 Error finish

S1908 Access conditions and access performance values for optimum access in the designated power consumption level are read from the card information storage part

S1909 Transmit read information to access device

Fig.20

S2001 Issue card type acquisition command

S2002 Card type acquisition successful?

S2003 Error finish

S2004 Card corresponding to access performance basic information list command?

S2005 Cancel access performance basic information list acquisition

S2006 Issue access performance basic information list

command

S2007 Acquisition of access performance basic information list successful?

S2008 Error finish

S2009 Calculate access rate value based on access performance basic information list

S2010 Determinate access condition based on access rate value

Fig.21

S2101 Receive command

S2102 Incorrect command?

S2103 Error finish

S2104 Optimum access performance basic information list acquisition command?

S2105 Perform other process

S2106 Read access performance basic information list from card information storage part

S2107 Transmit access performance basic information list to access device

Fig.22

(a) Access performance basic information list

Process contents

Reading

Writing

Erasing

(b) Processing time inside the card (e.g. busy time/512KB data transfer at writing processing)

Process unit size

Standard value

Sequential

Random

Worst value

Sequential

Random

Fig.23

(a)

Command line

Read commend

Response

Data line

Data

Data

Process inside card

Command interpretation

Reading read data

Reading read data

(b)

Command line

Write commend

Response

Data

Data

Data line

Busy

Busy

Process inside card

Command interpretation

Writing data

Writing data

Fig.24

Command line

Erase commend

Response

Data line

Busy

Process inside card

Command interpretation

Erase data

Fig.25

S2501 Issue card type acquisition command

S2502 Card type acquisition successful?

S2503 Error finish

S2504 Card corresponding to access performance table acquisition command

S2505 Cancel access performance table acquisition

S2506 Issue access performance table acquisition command

S2707 Acquisition performance table acquisition successful?

S2508 Error finish

S2509 Determinate access condition based on access performance table

Fig.26

S2601 Receive command

S2602 Incorrect command?

S2603 Error finish

S2604 Access performance table acquisition command?

S2605 Perform other process

S2606 Read access performance table from card information storage part

S2607 Transmit access performance table to access device

Fig.27

(a) Access performance table

Input clock

Process contents

Reading

Writing

Erasing

(b) Processable data size in unit time (e.g. input clock = 25MHz, kind of processing = writing)

Access unit

Standard value

Sequential

Random

Worst value

Sequential

Random

Fig.28

(a) Access performance table

Input clock

Process contents

Reading

Writing

Erasing

(b) Required time for unit size data processing (e.g. input clock = 25MHz, kind of processing = writing)

Access unit

Standard value

Sequential

Random

Worst value

Sequential

Random

Fig.29

Access performance table

Input clock

Process contents

Reading

Writing

Erasing

(b) Access performance as processing rate at the time of access in unit size (e.g. input clock = 25MHz, kind of processing = writing)

Access unit

Standard value

Sequential

Random

Worst value

Sequential

Random

Fig.30

117 Nonvolatile memory

Logical address

File system management area

3001 Management information area

3002 Data area

3003 Master boot record and partition table (MBR·PT)

3004 Partition boot sector (PBS)

3007 Route directory entry (RDE)

Fig.31

3001 Management information area

3002 Data area

Cluster#2 (Free)

Cluster#3 (Data 1)

Cluster#4 (Data 2)

Cluster#5 (Free)

Cluster#6 (Data 3)

Cluster#7 (Free)

FAT entry corresponding to cluster #2

Fig.32

S3201 Read directory entry

S3202 Confirm starting position of file

S3203 Read FAT and acquire a cluster number at a writing

position through a link

S3204 Acquisition of free area?

S3205 A free area is searched on FAT and allocate 1 cluster

S3206 Write data

S3207 Writing finished all data?

S3208 Write directory entry

S3209 Write FAT

Fig.33

(a)

3301 Directory entry

File name

Starting cluster number

File size

(b)

Corresponding cluster numbers

(c)

Cluster number 10

Cluster number 11

Cluster number 12

Cluster number 13

Cluster number 14

3002 Data area

Data 1 (Data start)

Data 2

Data 3

Data 4 (old data end)

Free area

1 cluster = 4096 Bytes

Fig.34

(a)

3301 Directory entry

File name

Starting cluster numbers

File size

(b)

Corresponding cluster numbers

(c)

Cluster number 10

Cluster number 11

Cluster number 12

Cluster number 13

Cluster number 14

3002 Data area

Data 1 (Data start)

Data 2

Data 3

Data 4

Data 5 (New data end)

1 cluster = 4096 Bytes

Fig.35

S3501 The file system control part requests acquisition of FS access unit to the access condition determination part

S3502 The access condition determination part requests acquisition of card information to the card information acquisition part

S3503 The card information acquisition part acquires card information from the semiconductor memory card

S3504 Success acquire?

S3506 Error finish

S3506 The card information acquisition part transmits card information to the access condition determination part

S3507 The access condition determination part acquires access conditions from the card use condition storage part

S3508 Determine an unit size suitable for the card use condition based on comparison between the card information and the card use condition

exists or not

S3509 Process unit size exists?

S3510 Error finish

S3511 Determine a suitable process unit size as FS

access unit and transmits the FS access unit from the access condition determination part to the file system control part

Fig.36

233 sector

1 sector

123 sector

123 sector

32 sector

1 cluster = 16KB

1006080 sector

Cluster#2

Cluster#3

Cluster#4

Cluster#5

Cluster#6

Cluster#7

Cluster#8

Cluster#9

3002 Data area

FS access unit 0 (128KB)

FS access unit 1 (128KB)

FS access unit 2 (128KB)

Management information area = Fs access unit × M

FS access unit = cluster × N

Fig.37

S3701 Is remaining data length more than FS access unit length?

S3702 Prepare data of FS access unit length

S3703 Acquire an area in which the area contained in the FS access unit consists of only free clusters is acquired

S3704 Does the area exist?

S3705 Error finish

S3706 Write data of the FS access unit length collectively on the acquired free area

S3707 Does all data writing finish?

S3708 Prepare remaining data

S3709 Acquire an area in which the area contained in the FS access unit consists of only free clusters

S3710 Does the area exist?

S3711 Error finish

S3712 Write the remaining data collectively on the acquired free area

Fig.38

FS access unit 0

FS access unit 1

FS access unit 2

```
      Cluster numbers
      3002  Data area
      Data 1 (FILE1)
      Data 2 (FILE1)
 5    Free
      Free
      Free
      Free
      Free
10    Free
      Directory 1 (DIR1)
      Directory 2 (DIR1)
      Free
      Free
15    Free
      Free
      Free
      Free
      Free
20    Free
      Free
      Free
      Free
      Free
25    Free
```

Free

New file data area

Fig.39

S3901 Set current search pointer for the first FSAU in data area

S3902 Does the directory area exist in the currently referred FS access unit?

S3903 Does a free cluster exist in the currently referred FS access unit?

S3904 Allocate the free cluster to the directory area

S3905 Does the confirmation of all area finish?

S3906 Set current search pointer for next FS access unit

S3907 Acquire an area in which the area contained in the FS access unit consists of only free clusters from the whole of the data area

S3908 Does the area exist?

S3909 Allocate a single free cluster contained in the acquired area to the directory area

S3910 Acquire free cluster from whole area

S3911 Does the area exist?

S3912 Error finish

S3913 Allocate the free cluster to the directory area

Fig.40

```
      FS access unit 0
      FS access unit 1
      FS access unit 2
      Cluster numbers
 5    3002  Data area
      Data 1 (FILE1)
      Data 2 (FILE1)
      Free
      Free
10    Free
      Free
      Free
      Free
      Directory 1 (DIR1)
15    Directory 2 (DIR1)
      Free
      Free
      Free
      Free
20    Free
      Free
      Free
      Free
      Free
25    Free
```

Free

Free

Free

Free

Management information storage area

Fig.41

FS access unit 0

FS access unit 1

FS access unit 2

Cluster numbers

3002 Data area

Data 1 (FILE1)

Data 2 (FILE1)

Free

Free

Free

Free

Free

Free

Directory 1 (DIR1)

Directory 2 (DIR1)

Free

Free

Free

Free

Free

Free

Directory 1 (DIR2)

Free

Free

Free

Data 1 (FILE2)

Free

Free

Data 2 (FILE2)

Fig.42

FS access unit 0

FS access unit 1

FS access unit 2

Cluster numbers

3002 Data area

Data 1 (FILE1)

Data 2 (FILE1)

Data 1 (FILE2)

Data 2 (FILE2)

Free

Free

Free

Free

Directory 1 (DIR1)

Directory 2 (DIR1)

Directory 1 (DIR2)

Free

Free

Free

Free

Free

Free

Free

Free

Free

Free

Free

Free

Free

Area for storing file data

Area for storing management information

Occur a free area of FE access unit length

Fig.43

S4301 Set 0 as the number of free FS access units

S4302 Set current search pointer for the first data area

S4303 Do all the clusters of the currently referred FS

access unit are free?

S4304 Add 1 to the number of free FS access units

S4305 Does confirmation of all area finish?

S4306 Set current search pointer for next FS access unit

S4307 Convert the free FS access unit number into the number of bytes, and inform the number to the application program

Fig.44

FS access unit

Cluster numbers

3002 Data area

Continuous free areas

Cluster numbers

Continuous free areas

Continuous free areas

Cluster in use

Free cluster

Fig.45

100 Access device

101 CPU

102 RAM

103 Slot

104 ROM

105 Application program

106 File system control part

107 Access condition determination part

108 Card information acquisition part

109 Access control part

110 card use condition storage part

111 Semiconductor memory card

4501 Semiconductor memory card control LSI

Fig.46

100 Access device

111 Semiconductor memory card

112 Host interface

113 CPU

114 RAM

115 ROM

119 Second memory

120 Logical-to-physical conversion control section

121 Free physical area generating section

123 Nonvolatile memory access section

125 Host information storage part

126 Address management information

127 User data

4601 Nonvolatile memory

4602 Memory controller

Fig.47

Logical sector address

Logical-to-physical conversion table

Physical sector address

Correspond to Nonvolatile memory tip A

Correspond to Nonvolatile memory tip B

Physical block address

Entry table

00: Valid block

11: Invalid block

10: Defective block

Fig.48

Sector number

Erase block

Data area (512byte)

Management area (16byte)

Fig.49

SA: Start sector address

L: Writing size (Sector unit)

Free block: Erase block

Main routine

(left)

Write to first half area only (nonvolatile memory tip A)

Sub routine 1

(right)

Write to latter half area only (nonvolatile memory tip B)

Sub routine 2

(middle)

Write access first half area (nonvolatile memory tip A) and latter half area (nonvolatile memory tip B)

Sub routine 2

Sub routine 1

(m×512B) >= 4KB

n=(m×512B)÷4KB (n= even number)

Write to free block of nonvolatile memory tip A

Erase n invalid blocks of nonvolatile memory tip B

Write to free block of nonvolatile memory tip A

Sub routine 2

(m×512B) >= 4KB

n=(m×512)÷4KB (n= even number)

Write to free block of nonvolatile memory tip B

Erase invalid blocks of nonvolatile memory tip A

Write to free block of nonvolatile memory tip B

Fig.50

Access to nonvolatile memory tip A

Write command issue period

Data transfer time

Program busy time

Writ 1

Write 2

Write 8

Access to nonvolatile memory tip B

Erase command issue period

Erase busy time

Fig.51

100 Access device

111 Semiconductor memory card

112 Host interface

113 CPU

114 RAM

115 ROM

119 Second memory

125 Host information storage part

126 Address management information

127 User data

5101 Nonvolatile memory

5102 Logical-to-physical conversion control section

5103 Nonvolatile memory access section

5104 Memory controller

Fig.52

Page (2112B)

Erase block (4224B)

Bus No=0

Bank 0

Bank 1

Bank 2

Bank 3

Nonvolatile memory tip A

Page No

Page No

Bank 0

Bank 1

Bank 2

Bank 3

Nonvolatile memory tip B

Logical section 0

Logical section 255

Fig.53

Logical address format

Logical section No

Page No

Bus No

Bank No

Sector No

Logical-to-physical conversion

Physical section No

Fig.54

Logical-to-physical conversion table

Logical section No.

Physical section No

Physical section No

Correspond to physical address of the erase block of bank 0 of the first nonvolatile memory chip A

Entry table

Physical block No.

00: Valid block

11: Invalid block

10: Defective block

Fig.55

Page 0

Page 1

Sector (512 bytes)

Data area (2048 bytes)

Management area (64 bytes)

Storage physical address information of 8 blocks in the section

Fig.56

Data transferred from access device 100 (Continuous logical addresses)

Bus No. 0

Write command

Data transfer period (A)

Program busy time (hatching)

Bus No. 1

Write command

Data transfer period (b)

Program busy time (hatching)

Fig.57

Data transferred from access device 100 (Continuous logical addresses)

Waiting period for data transmission to the host (card busy period)

Bus No. 0

Write command

Data transfer period (A)

Program busy time (hatching)

Bus No. 1

Program complete signal

(Continue the below)

(Continue the above)

Fig.58

100 Access device

111 Semiconductor memory card

112 Host interface

113 CPU

114 RAM

115 ROM

118 First memory

119 Second memory

124 Card information storage part

125 Host information storage part

126 Address management information

127 User data

5801 Nonvolatile memory

5802 Logical-to-physical conversion control section

5803 Nonvolatile memory access section

5804 Memory controller

Fig.59

5801 Nonvolatile memory

Page (528B)

Erase block (16896B)

Bank 0

Bank 1

Bank 2

Bank 3

Fig.60

(a)

Logical address

Logical-to-physical conversion table

Selector

Physical address

Logical-to-physical conversion through flag

(b)

Physical block address

Entry table

00: Valid block

11: Invalid block

10: Defective block

Fig.61

Logical block address

Logical-to-physical conversion table

Physical block address

Fig.62

100 Access device

111 Semiconductor memory card

112 Host interface

113 CPU

114 RAM

115 ROM

119 Second memory

125 Host information storage part

126 Address management information

127 User data

2101 Nonvolatile memory

6202 Logical-to-physical conversion control section

6203 Free physical area generating section

6204 Nonvolatile memory access section

6205 Memory controller

Fig.63

(a)

Logical sector address

Logical-to-physical conversion table

Physical selector address

Physical block address

(b)

Entry table

000: Valid block

011: Invalid block

010: Defective block

001: Free block (erased block)

100: Brock to be defragmented

Fig.64

Sector number

Erase block 1

Logical sector 4 New

Logical sector 0 Old

Logical sector 0 New

Logical sector 1 New

Logical sector 3 New

Logical sector 2 New

Sector number

Erase block 5

Logical sector 10 Old

Logical sector 18 Old

Logical sector 10 New

Logical sector 11 New

Erase block 9

Logical sector 0 New

Logical sector 1 New

Logical sector 2 New

Logical sector 3 New

Logical sector 10 New

Logical sector 11 New

Sector number

Fig.65

100 Access device

111 Semiconductor memory card

112 Host interface

113 CPU

114 RAM

115 ROM

119 Second memory

125 Host information storage part

126 Address management information

127 User data

6501 Nonvolatile memory

6502 Logical-to-physical conversion control section

6503 Nonvolatile memory access section

6504 Memory controller

Fig.66

Erase block

Data area

AT area

Fig.67

Memory bus

Read command

AT transfer period

Write command

Data transfer period

Program busy period

Write command

Data transfer period

Program busy period

AT read

Data write

AT write

Fig.68

Memory bus

Read command

AT transfer period

Write command

Data transfer period

Program busy period

Write command

Data transfer period

Program busy period

Write command

Data transfer period

Program busy period

AT read

Data write

Data write

AT write

AT update instruction signal

[Title of the Document] ABSTRACT

[ABSTRACT]

[Object] The present invention aims at allowing access device to make fast access to semiconductor memory card whose access condition and access performance vary according to characteristics and management method of semiconductor memory for use.

[Means to solve the problem] Card information storage part 124 is provided in semiconductor memory card 111 to store information on characteristics including access condition and access performance of semiconductor memory card 111. Access device 100 acquires stored information from semiconductor memory card 111 for use in file system control. This optimizes process operations in access device 100 and semiconductor memory card 111 thereby to achieve fast access to semiconductor memory card 111.

[Selected Figure] Figure 1